



EECE 379 : Digital and Microcomputer System Design

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Instructor

Ed Casas. Contact me by e-mail (edc@ee.ubc.ca) or come by my office in MCLD 451 (822-2592). Most questions about the course should be posted to the course mailing list.

Lectures and Tutorials

Monday, Wednesdays and Fridays, 12:30 AM to 1:20 PM in MCLD 402. Lectures begin September 6 and end December 1. Tutorials will cover new and important material and attendance is required.

Labs

Lab Schedule

Alternate weeks, in MCLD 254. You must register through Telereg for one of the four sections. Sections A and B are on Tuesdays from 9:30 AM to 12:30 PM while sections C and D are on Mondays from 2:30 to 5:30 PM.

To switch lab sections: (1) Find someone willing to change into the section you are currently registered for (you can use the course mailing lists for this), and (2) both persons must notify the lab TAs by e-mail. Since there are (almost) no free lab spaces available you *must* show up for your scheduled lab period.

The lab sections are scheduled as follows:

	Lab 1	Lab 2	Lab 3	Lab 4
Mon	Sep 18 - D	Oct 16 - D	Oct 30 - D	Nov 20 - C
Tue	Sep 19 - A	Oct 17 - A	Oct 31 - A	Nov 21 - B
Mon	Sep 25 - C	Oct 23 - C	Nov 6 - C	Nov 27 - D
Tue	Sep 26 - B	Oct 24 - B	Nov 7 - B	Nov 28 - A

Please note that the lab schedule is irregular due to holidays.

Lab Procedure

Labs are to be done individually. Many students find that completing all of the labs is the most difficult part of this course.

For most labs you will not have enough time to design, build and debug your circuit during the lab. Therefore, you must design and verify your solution (through simulation) before coming to the lab. You will be required to hand in the source code

and correct simulation results before starting the lab.

You must print out the revised source code (VHDL and/or assembler) and demonstrate your working design to the TA before the end of the lab session. The TA will then ask one or two questions about your program to make sure you understand the material. If did your own work you shouldn't have any problems answering the question(s).

A short lab report must be handed in to the course assignment box (see below) before the start of your next lab on the dates shown above. This report should include a brief description of your design, source code listings, schematics or block diagrams, and answers to any questions posed in the lab notes. Lab reports should be placed in the box marked "EECE 379 Assignments" outside MCLD 332.

Lab Marking

Each lab will be marked out of 6 as follows:

complete, simulated and correct pre-lab	1
a program and/or circuit that works properly	3
correct answers to questions after demo	1
accurate, complete and well-written report	1

Note: If a working circuit is not demonstrated by the end of the scheduled lab session you will receive a mark of zero for the second component (0/3). If you do not complete the lab on time hand in a report describing your simulated circuit. If the report is not handed in on time you will receive zero for the report (0/1).

You must complete all four labs to pass the course. All four lab marks will count towards your final mark.

Plagiarism

Each student must submit an original solution. Possible penalties for plagiarism include a mark of zero for all labs.

Assignments

Several assignment will be given out during the term and will be due one week later. Solutions will be given out for all questions but not all questions will be marked. *Late assignments will be given a mark of zero.* Assignments should be placed in the same box used to hand in the lab reports (the box marked "ELEC 379 Assignments" outside MCLD 332. The TAs will separate out the labs from the assignments. Please do *not* assignments in at lectures.

Assignments are to be done individually. Students are encouraged to seek help from classmates but copying is not allowed. Possible penalties for plagiarism include a mark of zero for all assignments.

Bonus marks may be awarded for the fastest, the smallest and the most readable (as judged by the TA) designs submitted for each assignment.

Teaching Assistants

Louis Hong (lhong@ee.ubc.ca) and Peter Hallschmid (peterh@ee.ubc.ca) will supervise the labs and Tony Wong (tonyw@ece.ubc.ca) will mark the assignments.

Web Page

The course Web page (<http://casas.ee.ubc.ca/379>) will be used to make announcements and to distribute course material (e.g. data sheets). You can also use the Web page to check your marks and view the course mailing list archives. Any web browser can read these pages.

The lecture notes, assignments, labs and solutions will be available from the Web page in PDF and other formats. Free software to view and print PDF documents (Ghostview, xpdf, Adobe Acrobat Reader) is available for most computers.

Mailing List

The lecturer will post important announcements about the course on the `eece379-announce` mailing list. All students in the course should subscribe to this mailing list.

Students should post questions or answers about the course material to the `eece379` mailing list.

Instructions on subscribing are available on the course Web page.

The mailing lists can also be accessed through the `eece379-announce` and `eece379` archives.

Text

We will not use a textbook in this course. Concepts will be explained in the lecture notes and we will use manufacturers' data sheets and standards documents as examples and reference material. I hope this will give you a better introduction to the design process than using a textbook.

Detailed notes will be distributed before the relevant lecture. The notes will often contain exercises or sections to be completed during the lecture.

Please wait until the end of the lecture before taking extra copies. You can always print copies from the course's Web page (see below).

Other References

The lecture notes and Web references will cover the subset of digital logic design, VHDL and the 80x86 architecture that we will need. However, a number of textbooks and references are available if you would like to learn more:

- *Contemporary Logic Design* by Katz, Addison Wesley, 1993. Is the EECE 259 textbook and covers some of the material on logic design. If you already have that textbook you may wish to refer to it for alternative explanations of various topics.
- *VHDL for Logic Synthesis: An Introductory Guide for Achieving Design Requirements*, Second Edition, by Andrew Rushton (McGraw-Hill, 1998, \$98) is a concise guide to logic synthesis using VHDL.
- *VHDL Made Easy* by David Pellerin and Douglas Taylor (Prentice-Hall, 1997), \$91, is an easy-to-read introduction to using VHDL for design.
- *The Designer's Guide to VHDL* by Peter J Ashenden (Morgan Kaufmann, 1996) is an complete reference on the VHDL language.
- *The 80x86 Family* by John Uffenbeck (Prentice-Hall, 1998) covers the 80x86 family of microprocessors and their support chips in detail.
- *The Indispensable PC Hardware Book*, third edition, by Hans-Peter Messmer (Addison-Wesley, 1997), \$59, is a detailed reference on the IBM PC Architecture.
- *The Art of Electronics*, second edition, by Paul Horowitz and Winfield Hill, Cambridge University Press, 1989, \$100, is a good practical reference book on most aspects of electronics although much of the material is now dated.

These books cover much more than you will need for this course. A number of tutorials and a short book on VHDL are available on the net (see the Web page).

Evaluation

There will be a 50-minute mid-term examination on Friday, October 20 from 12:30 to 1:20 PM and a 3-hour final exam in December. The final mark will be calculated as follows:

final exam	49%
midterm exam	20%
assignments	10%
labs	20%
participation	1%

You must also complete all four labs to pass the course.

The participation mark will be awarded (at the end of the course) to students that asked or answered a non-trivial question on the course mailing list. Please include an approximation of your real name (but *not* your student number) when posting to the mailing list.

Changes to the marking scheme will require the agreement of the instructor and *all* of the students.

Software

The Altera MaxPlusII VHDL synthesis and simulation software will be available on the department's PC and Sun networks and you may also install it on your PC (MS-Windows 3.11, 95 or NT) if you wish.

A free 80x86 assembler is available on the course Web page and on the department's PCs.

Intended Audience

Students who will design systems that include digital electronics.

EECE 379 is designed for students in the Electrical Engineering rather than the Computer Engineering stream. The course covers the same material as a combination of EECE 353 (logic design) and EECE 465 (microcomputer design) but does not cover the material in as much depth.

If you are in the computer engineering option you should probably take EECE 353 plus EECE 465 rather than this course. Ask your faculty advisor for more details.

Prerequisites

Student should have experience in designing simple digital circuits and in assembly-language programming.

Objectives

By the end of the course the student should have the background required to begin designing microprocessor-based systems using programmable logic ICs. In general, the student should be able to:

- design and test combinational and sequential logic circuits using the synthesis subset of VHDL covered in the course
- give the values of the 80386 data, address and control bus signals during read or write cycles to I/O or memory
- describe the steps carried out by an 8088 processor in response to an interrupt
- select the appropriate type of memory device for a given application (SRAM, ROM, DRAM, flash EEPROM, etc)
- draw schematics of multi-chip memories for a given memory chip, data bus width and address range
- compute margins for read and write cycles using CPU and memory data sheet timing diagrams and specifications
- select and justify the choice of I/O strategy (polling or interrupt-driven; programmed I/O or DMA) for a given application
- write software to control programmable peripherals (e.g. DMA controllers, interrupt controller, timer/counter, parallel and serial interfaces) in 80x86

- assembly language by reading and writing status, control, and data registers
- describe and analyze the behaviour of “RS-232” and SCSI bus signals during common operations

Detailed objectives will be provided in the introduction to each set of lecture notes.

Course Outline

The course is structured in a bottom-up order: digital logic circuits, the processor bus, the system bus, and peripheral interfaces. As examples we will use Altera 10K FPGAs, the Intel 80386 CPU, the ISA/PC-104 and PCI system buses and RS-232 and SCSI peripheral interfaces.

- review of digital logic design
- logic synthesis with VHDL
- the 80386 microprocessor
- memory system design
- polled, interrupt-driven and DMA interfaces
- system buses (ISA, PCI)
- peripheral buses (Serial, Centronics, SCSI)

Related Courses

This course deals with the design of digital logic circuits, primarily those involving microprocessors. Related topics that are not covered in this course include:

- CPU design is covered in EECE 476.
- IC design is covered in EECE 479.
- operating systems are covered in CPSC 415 or ELEC 494.