Solution to Assignment 4
Memory Design and Timing Analysis

Question 1

RAM Design

1. *chips per bank*: To create a 16-bit wide data bus using 8-bit chips we need $16/8 = 2$ chips per bank.

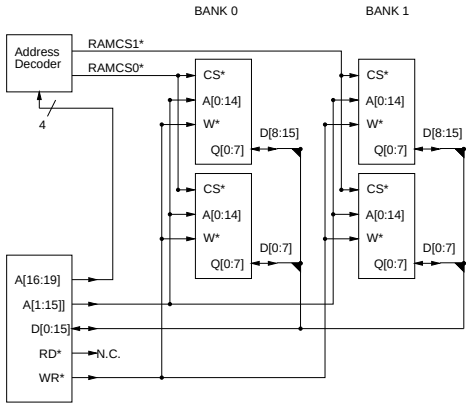
2. *number of banks*: Using a total of 4 chips and putting 2 chips/bank we can assemble $4/2 = 2$ banks. Since each bank provides 32 k words of 2 bytes/word the total is $32 \times 2 = 64$ k bytes per bank. This provides a total of 128k bytes of RAM.

3. *byte-select address lines*: To select from the 2 bytes available in parallel we need to use the $\log_2 2 = 1$ least-significant CPU address bit (A0).

4. *word-select address lines:* To select one word in each bank we need $\log_2 32\text{k} = 15$ address bus bits (A1 to A15).

5. *bank-select address lines:* The remaining ($20 - 16 = 4$) address lines (A16 to A19) are then used to select a bank.

The schematic of the RAM design is:



EPROM Design

1. *chips per bank*: To create a 16-bit wide data bus using 4-bit chips we need $16/4 = 4$ chips per bank.

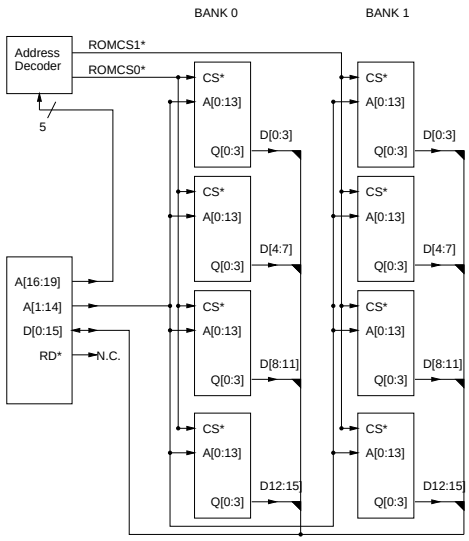
2. *number of banks*: Using a total of 8 chips and putting 4 chips/bank we can assemble $8/4 = 2$ banks. Since each bank provides 16 k words of 2 bytes/word the total is $16 \times 2 = 32$ k bytes per bank. This provides a total of 64k bytes of RAM.

3. *byte-select address lines*: To select from the 2 bytes available in parallel we need to use the $\log_2 2 = 1$ least-significant CPU address bit (A0, not available outside the CPU).

4. *word-select address lines:* To select one word in each bank we need $\log_2 16\text{k} = 14$ address bus bits (A1 to A14).

5. *bank-select address lines:* The remaining ($20 - 15 = 5$) address lines (A16 to A19) are then used to select a bank.

The schematic of the EPROM design is:



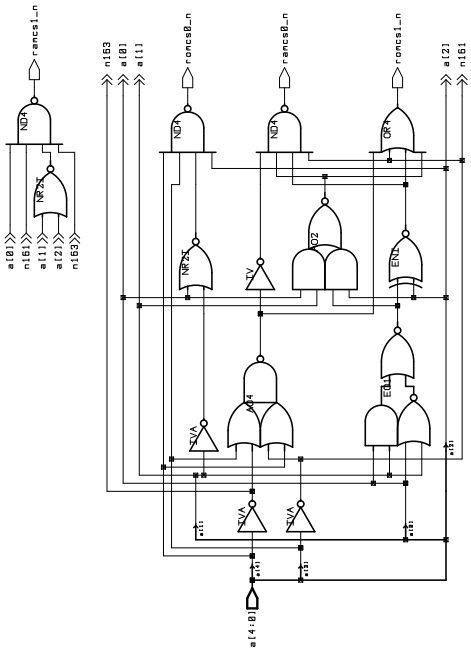
Question 2

```
library ieee ;
use ieee.std_logic_1164.all ;

entity decoder is
   port (
   a : in std_logic_vector (4 downto 0) ;
   ramcs0_n, ramcs1_n : out std_logic ;
   romcs0_n, romcs1_n : out std_logic ) ;
end decoder ;

architecture rtl of decoder is
begin
   ramcs0_n <= '0' when a = "00000" else '1' ;
   ramcs1_n <= '0' when a = "00001" else '1' ;
   romcs0_n <= '0' when a = "11110" else '1' ;
   romcs1_n <= '0' when a = "11111" else '1' ;
end rtl ;
```

The synthesized schematic for this design is:



Question 3

Timing Specifications

In the tables below I've used the following abbreviations:

symbol	meaning
S	guaranteed timing response
R	timing requirement
C	CLK2 period (40 ns)
W_{min}	minimum width
W_{max}	maximum width
PD	propagation delay

Note that if the margin is zero the specification is met.

CPU Write Cycle

All the signals are outputs.

	R/S	type	value	from	to
t_{41}	S	W_{min}	0	address	WR*
t_{41a}	S	W_{min}	0	CS*	WR*
t_{42}	S	W_{min}	0	WR*	address
t_{42a}	S	W_{min}	0	CW*	CS*
t_{42b}	S	W_{min}	10	WR*	address
t_{43}	S	W_{min}	2C-10	data	WR*
t_{44}	S	W_{min}	C-10	WR*	data
t_{45}	S	W_{max}	C+10	WR*	data
t_{46}	S	W_{min}	2C-10	WR*	WR*

CPU Read Cycle

All signals except data bus are outputs.

	R/S	type	value	from	to
t_{47}	R	W_{max}	4C-41	address	data
t_{47a}	R	W_{max}	4C-42	CS*	data
t_{48}	R	W_{max}	3C-39	RD*	data
t_{49}	R	W_{min}	0	RD*	data
t_{50}	R	W_{max}	C	RD*	data
t_{51}	S	W_{min}	0	RD*	address
t_{51a}	S	W_{min}	0	RD*	CS*
t_{52}	S	W_{min}	3C-13	RD*	RD*

RAM Read Cycle

All signals except data bus are inputs.

	R/S	type	value	from	to
t_{RC}	R	W_{min}	70	address	address
t_{AA}	S	PD	70	address	data
t_{CO1}	S	PD	70	CE1*	data
t_{CO2}	S	PD	70	CE2	data
t_{OH}	S	PD	10	address	data
t_{LZ1}	S	PD	10	CE1*	data
t_{LZ2}	S	PD	10	CE2	data
t_{HZ1}	S	PD	30	CE1*	data
t_{HZ2}	S	PD	30	CE2	data

RAM Write Cycle

All signals are inputs except data bus for t_{WHZ} and t_{OW}). The RAM write cycle is WE* controlled (Chart 1) because the CPU timing specifications show that WE* (WR*) goes active after CE1* (CS1*).

	R/S	type	value	from	to
t_{WC}	R	W_{min}	70	address	address
t_{CW1}	R	W_{min}	50	CE1*	CE1*
t_{CW1}	R	W_{min}	60	CE2	CE2
t_{AW}	R	setup	50	address	WE*
t_{WP}	R	W_{min}	55	WE*	WE*
t_{DW}	R	setup	30	data	WE*
t_{DH}	R	hold	0	WE*	data
t_{AS}	R	W_{min}	0	address	WE*
t_{WR}	R	hold	0	WE*	address
t_{WHZ}	S	PD	30	WE*	data
t_{OW}	S	PD	10	WE*	data

Flash Read Cycle

All signals except data bus are inputs.

	R/S	type	value	from	to
t_{RC}	R	W_{min}	80	address	address
t_{ACE}	S	PD	80	CE*	data
t_{AOE}	S	PD	40	OE*	data
t_{AA}	S	PD	80	address	data
t_{OD}	S	PD	20	OE*, CE*	data
t_{OH}	S	PD	0	OE*, CE* address	data

Timing Analysis

We only need to verify that timing *requirements* are met.

CPU Requirements - RAM Read Cycle

Since RD* is not connected to the RAM, the CPU timing requirements relative to RD* cannot be checked.

	required	expression	margin
t_{47}	4C-41 = 119	t_{AA} = 70	49
t_{47a}	4C-42 = 118	t_{CO1} = 70	48
t_{48}	3C-39 = 81	unknown	
t_{49}	0	unknown	
t_{50}	C = 40	unknown	

CPU Requirements - Flash Read Cycle

	required	expression	margin
t_{47}	4C-41 = 119	t_{AA} = 80	39
t_{47a}	4C-42 = 118	t_{ACE} = 80	38
t_{48}	3C-39 = 81	t_{AOE} = 40	41
t_{49}	0	t_{OH} = 0	0
t_{50}	C = 40	t_{OD} = 20	20

RAM Requirements - CPU Read Cycle

	required	expression	margin
t_{RC}	70	4C = 160	90

RAM Requirements - CPU Write Cycle

	required	expression	margin
t_{WC}	70	4C = 160	90
t_{CW1}	50	$t_{41a} + t_{46}$ = 70	20
t_{CW2}	50		
t_{AW}	50	$t_{41} + t_{46}$ = 70	20
t_{WP}	55	t_{46} = 70	15
t_{DW}	30	t_{43} = 70	40
t_{DH}	0	t_{44} = 30	30
t_{AS}	0	t_{41} = 0	0
t_{WR}	0	t_{42} = 0	0

Flash Requirements - CPU Read Cycle

	required	expression	margin
t_{RC}	80	4C = 160	80