Assignment 4
Memory Design and Timing Analysis

due Friday, November 24, 2000

Question 1

Draw the schematic of a memory system using RAM and EPROM for a 16-bit CPU using four 32k by 8 SRAMs and eight 16k by 4 EPROMs. The CPU uses conventional byte addressing with each byte addressable. However, assume the CPU always reads or writes 16 bits at a time (no byte selects required) and has a 20-bit address bus (of which only `A1` to `A19` available), a 16-bit data bus (`D0` to `D15`) and `RD*` and `WR*` read/write signals. Each memory chip has bi-directional data in/out pins (`Q0` to `Q7` or `Q0` to `Q3`), address inputs (`A0`, `A1`, ...) and an active-low chip-select signal (`CS*`). The RAMs also have active-low write strobes (`W*`). The `CS*` pins should be driven from an address decoding circuit and W* should be driven from the CPU's `WR*` signal. You may assume all memory chips' outputs are tri-stated when the `CS*` is not asserted. Show all connections between the CPU and the memory chip pins.

You may use the bus notation `X[n:m]` to indicate a subset of the signals of `X` consisting of bits n through m. For example, the following diagram shows that `D2` connects to `Q6` and `D3` connects to `Q7`:

To avoid ambiguity, place pin (signal) labels inside the rectangles representing the chips and the corresponding bus labels outside.

The details of the address decoders need not be shown.

Question 2

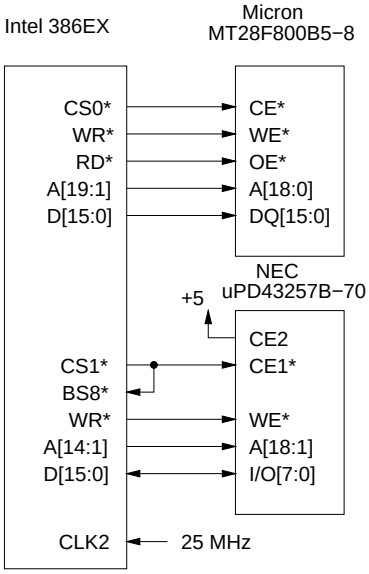
Design an address decoders for the circuit described above as a synthesizable circuit description in VHDL.

The decoders should place the RAM starting at memory location 0 and the EPROM at memory location F0000H. The decoders should fully decode CPU addresses.

Write an entity and an architecture. Use `std_logic_vector`-type input signal named `A` with an appropriate `downto` range and as many active-low `std_logic`-type outputs signals named `ROMCSi_N` and `RAMCSi_N` (i=0,1,...) as are required by your design. You need not synthesize or simulate your design.

Question 3

In this assignment you will perform a complete timing analysis on a simple microcomputer system. The design you are to analyze consists of: (1) an Intel 386EX microprocessor (2) an NEC μPD43257B-70 32k $\times$ 8 SRAM, and (3) a Micron MT28F800B5 512K $\times$ 16 'flash' EEPROM connected as follows:



Assume the supply voltage is above 3.0 volts and use the 25 MHz CLK2 specifications. Note that a CPU cycle takes 4 CLK2 cycles or 160 ns if CLK2

is 25 MHz. This value should be used as the cycle time.

Note that although some output-to-input minimum width specifications are labelled setup or hold requirements in the CPU specifications, the true setup/hold requirements are measured to an input signal, CLK2. These requirements appear in a earlier part of the table (e.g. t_{21} and t_{22}) and will be met if the "higher level" requirements given below are met.

The data sheets for these devices are available in PDF format at the following URLs. To do this assignment you'll only need to print out the pages containing the timing specifications and diagrams from each data sheet as shown below (you can, of course, print out more if you want to learn more about the devices).

- `ftp://download.intel.com/design/intarch/DATASHTS/27242007.pdf` (Pages 38, 39 and 46).
- `http://www.ic.nec.co.jp/memory/pdfs/M10693EJ7V0DS00.pdf` (Pages 8, 9 and 10).
- `http://www.micron.com/flash/pdfs/Q11_2.pdf` (Pages 4, 21 and 22).

The 386EX read and write cycles are the same as those of the 386SX. However, the 386EX (which is the chip used in the lab SBC) is designed to be used in control applications and several common peripherals have been integrated into the chip. These include six address decoders (the CSx outputs) and the logic for generating separate active-low read and write strobes (RD* and WR*).

From the timing diagram and your understanding of CPU bus cycles prepare a table identifying each CPU timing specification from t41 to t52 (inclusive) as a guaranteed response or a timing requirement. Also classify each specification as a propagation delay, setup time, hold time, maximum frequency, or a minimum width (choose the closest if none fit exactly). Repeat for the RAM read and write cycle specifications (pages 8 and 9) and for the flash read cycle specifications (page 21, omit the two specifications involving RP*).

Perform a timing analysis for three types of cycles: RAM read, RAM write and flash read (word). For each cycle, obtain an *equation* for each timing requirement as a function of the guaranteed responses and the clock periods (assume CLK2 is 25 MHz) and then compute the margin available for each requirement (negative if the requirement is not met). For each requirement that is not met, find the number of additional wait (T2) states that would have to be inserted so that the requirement would be met. Note any requirements where it is not possible to determine if the requirements are met.

Your results should be presented as four tables: one classifying the timing specifications and one for each timing analysis.