Course Information

Instructor

Ed Casas. You can contact me by e-mail (edc@ee.ubc.ca) or at my office in MCLD 451 (822-2592), preferably during office hours.

Office Hours

Day/time to be decided (see the course Web page for the latest information).

Lectures and Tutorials

Monday, Wednesday and Friday, 8:30 to 9:20 AM in MCLD 402. Tutorials cover new and important material and attendance is required.

Assignments

Assignments will be given out approximately once a week and will be due one week later. Solutions will be given out for all questions but not all questions will be marked. *Late assignments will be given a mark of zero.*

Assignments are to be done individually. Students are encouraged to seek help from classmates but copying is not allowed. Possible penalties for plagiarism include a mark of zero for all assignments.

Bonus marks may be awarded for the fastest, the smallest and the most readable (as judged by the TA) designs submitted for each assignment.

Labs

Alternate Thursdays, in MCLD 254. You must register through Telereg for one of the three sections. Sections A and B are from 11:30 to 2:30 while section C is from 8:30 to 11:30. Lab sections A and C will start January 14. See the Web page for the latest schedule.

All labs are to be done individually.

All labs require that you design and simulate a circuit before the lab. You will be required to hand in a simulated design before starting the lab.

You must print out the source code (VHDL and/or assembly language) and demonstrate your working design to the TA before the end of the lab session. The TA will then ask you one or two questions about your program to make sure you understood the material covered by the lab. If did your own work you shouldn't have any problems answering the question(s).

A short lab report must be handed in to the course assignment box (see below) before 9:30 AM on the due dates (see the Web page, typically the due date is the date of your next lab). This report should include a brief description of your design, source code listings and schematics, and answers to any questions posed in the lab notes.

Each lab will be marked out of 5 as follows:

complete pre-lab design	1
correct program/circuit	2
answers after demo	1
accurate/complete/neat report	1

Come to the lab prepared! You should make sure your design compiles and simulates properly or you are unlikely to finish the lab in time. If a lab is not demonstrated by the end of the alloted time you will receive zero for completing the lab (0/2).

If the report is not handed in on time you will receive zero for the report (0/1).

You must complete all labs to pass the course – even if you would get a mark of zero for a lab.

Each student must submit an original solution. Possible penalties for plagiarism include a mark of zero for all labs.

Evaluation

There will be a 50-minute mid-term examination in late February (date TBD) and a three-hour final exam in April. The final mark will be calculated as follows:

final exam	50%
midterm exam	25%
labs	15%
assignments	10%

Note: You must complete all of the labs to pass the course.

Teaching Assistants

See the Web page for names and e-mail addresses. The TAs will mark assignments and supervise the labs.

Web Page

The course Web page:

`http://casas.ee.ubc.ca/379`

will be used to make announcements and to distribute course material (e.g. data sheets). You can also use the Web page to check your marks. Any browser can be used read these pages.

The lecture notes, assignments, labs and solutions will be available from the Web page in PDF format. Free software to view and print PDF documents (Adobe Acrobat) is available for most computers.

Software

The Altera MaxPlusII VHDL synthesis and simulation software will be available on the department's PC and Sun networks and you may also install it on your PC (MS-Windows 3.11, 95 or NT) if you wish.

A free 80x86 assembler will be available on the course Web page.

Intended Audience

Students who will design systems that include digital electronics.

ELEC 379 is a course designed for students in the Electrical Engineering rather than the Computer Engineering stream. The course covers the same material as a combination of ELEC 353 (logic design) and ELEC 465 (microcomputer design) but does not cover the material in as much depth.

If you are in the computer engineering option you should probably take ELEC 353 plus ELEC 465 rather than this course. Ask your faculty advisor for more details.

Prerequisites

Student should have experience in the design of simple digital circuits and have done some machine language programming of a microprocessor.

Text

You will not need a textbook for this course. Concepts will be explained in the lecture notes and we will use manufacturers' data sheets and standards documents as examples and reference material. I hope this will give you a better introduction to the design process than using a textbook.

Detailed notes will be distributed before the relevant lecture. The notes will often contain exercises or sections to be completed during the lecture.

Please wait until the end of the lecture before taking extra copies. You can always print copies from the course's Web page.

Other References

Much of the material on logic design is covered in the ELEC 259 textbook (Katz : Contemporary Logic Design, Addison Wesley, 1993) and if you already have that textbook you may wish to refer to it for alternative explanations of various topics.

The lecture notes and Web references will cover the small subset of the VHDL language that we will need. However, a number of texbooks and references are available if you would like to learn more about logic synthesis with VHDL. *VHDL for Logic Synthesis: An Introductory Guide for Achieving Design Requirements* by Andrew Rushton (McGraw-Hill, 1996) is a good text on logic synthesis using VHDL. *VHDL Made Easy* by David Pellerin and Douglas Taylor (Prentice-Hall, 1997) is an easy-to-read introduction to using VHDL for design. *The Designer's Guide to VHDL* by Peter J. Ashenden (Morgan Kaufmann, 1996) is an complete reference on the VHDL language. These books cover much more than you will need for this course. A number of tuto-

rials and a short book on VHDL are available on the net (see the Web page).

The Indispensable PC Hardware Book, third edition, by Hans-Peter Messmer (Addison-Wesley, 1997) is a detailed reference on the IBM PC Architecture.

The Art of Electronics, second edition, by Paul Horowitz and Winfield Hill (Cambridge University Press, 1989) is a good practical reference book on most aspects of electronics although much of the material is now outdated.

Objectives

By the end of the course the student should have the background required to design microprocessor-based systems using programmable logic ICs. The student should be able to:

- design and test combinational and sequential logic circuits using the synthesis subset of VHDL covered in the course
- give the values of the 80386 data, address and control bus signals during read or write cycles to I/O or memory
- describe the steps carried out by an 8088 processor in response to an interrupt
- select the appropriate type of memory device for a given application (SRAM, ROM, DRAM, flash EEPROM, etc)
- draw schematics of multi-chip memories for a given memory chip, data bus width and address range
- compute margins for read and write cycles using CPU and memory data sheet timing diagrams and specifications
- select and justify the choice of I/O strategy (polling or interrupt-driven; programmed I/O or DMA) for a given application
- write software to control programmable peripherals (e.g. DMA controllers, interrupt controller, timer/counter, parallel and serial interfaces) in 80x86 assembly language by reading and writing status, control, and data registers
- describe and analyze the behaviour of "RS-232" and SCSI bus signals during common operations

Detailed objectives will be provided in the introduction to each set of lecture notes.

Course Outline

The course is structured in a bottom-up order: digital logic circuits, the processor bus, the system bus, and peripheral interfaces. As examples we will use Altera 10K FPGAs, the Intel 80386 CPU, the ISA/PC-104 and PCI system buses and RS-232 and SCSI peripheral interfaces.

- review of digital logic design and logic synthesis with VHDL
- the 80386 microprocessor bus
- memory system design
- timing analysis
- polled, interrupt-driven and DMA interfaces
- system buses (ISA, PCI)
- peripheral buses (serial, SCSI)

Related Courses

This course deals with the design of digital logic circuits, primarily those involving microprocessors. Related topics that are not covered in this course include:

- CPU design is covered in ELEC 476.
- IC design is covered in ELEC 479.
- operating systems are covered in CPSC 415 or ELEC 494.