THE UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ELEC 379 : Design of Digital and Microcomputer Systems
1998/99 Winter Session Term 2

FINAL EXAMINATION
8:30 AM – 11:30 AM
January 23, 1999

This exam has five (5) questions. The marks for each question are as indicated. There are a total of 70 marks. Answer all questions. Write your answers in the exam book provided. Show your work. You may answer the questions in any order. Books, notes and calculators are allowed. You may keep this exam paper.

Question 1 (15 marks)

This question asks you to design a device that performs a binary search for an unknown value.

The device has the following VHDL entity declaration:

```
library ieee ;
use ieee.std_logic_1164.all ;
use ieee.std_logic_arith.all ;

entity SAR is
   port (
      test_out : out std_logic_vector (7 downto 0) ;
      done : out std_logic ;
      high, reset, clk : in std_logic ) ;
end SAR ;
```

This device has two internal 8-bit registers: `test` and `delta`.

On each rising edge of the clock if `reset` is '1' your design should set `test` to 128 and `delta` to 64.

On each rising edge of the clock if `reset` is not '1' your circuit should do the following:

- if `high` is '1' it should subtract `delta` from `test` otherwise it should add `delta` to `test`, and
- divide the value of `delta` by two.

The `done` output should be set to '1' only when `delta` is 0.

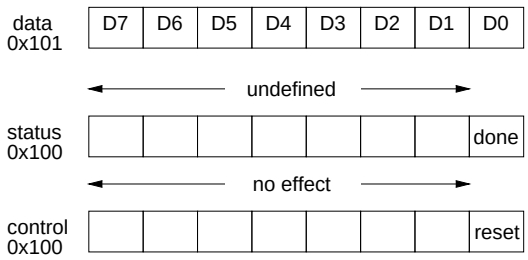
Write an architecture that implements this device and is synthesizeable by MaxPlus+II. Use type conversion functions as necessary. Any `process` in your VHDL code must contain

exactly one `if` statement surrounding one or two simple signal assignments. You need not include comments, `library` or `use` statements.

Hints: use "-" or "+". MaxPlus+II allows you to divide `unsigned` *values by 2.*

Question 2 (14 marks)

Write a subroutine, `sample:`, in 8086 assembly language that reads 200 (decimal) bytes from a peripheral and saves the bytes to a buffer. The peripheral is accessed through an 8-bit input data register at I/O (not memory) address 101H, an 8-bit status register at I/O address 100H and an 8-bit control register also at address 100H:



Before reading each byte from the data register your program must do the following:

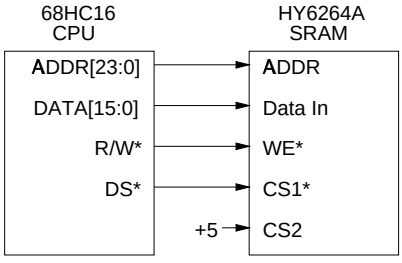
- write a 1 to the least significant (LS) bit of the control register, and
- wait until the LS bit of the status register is '1'.

Note that the other bits of the status register are undefined and only the LS bit of the control register has any effect.

Your function must save and restore any registers it modifies before returning control to the calling function with a `RET` instruction. You must declare storage for any variables you use (including the buffer), but you need not include comments or assembler directives such as `segment`, `assume` or `org`.

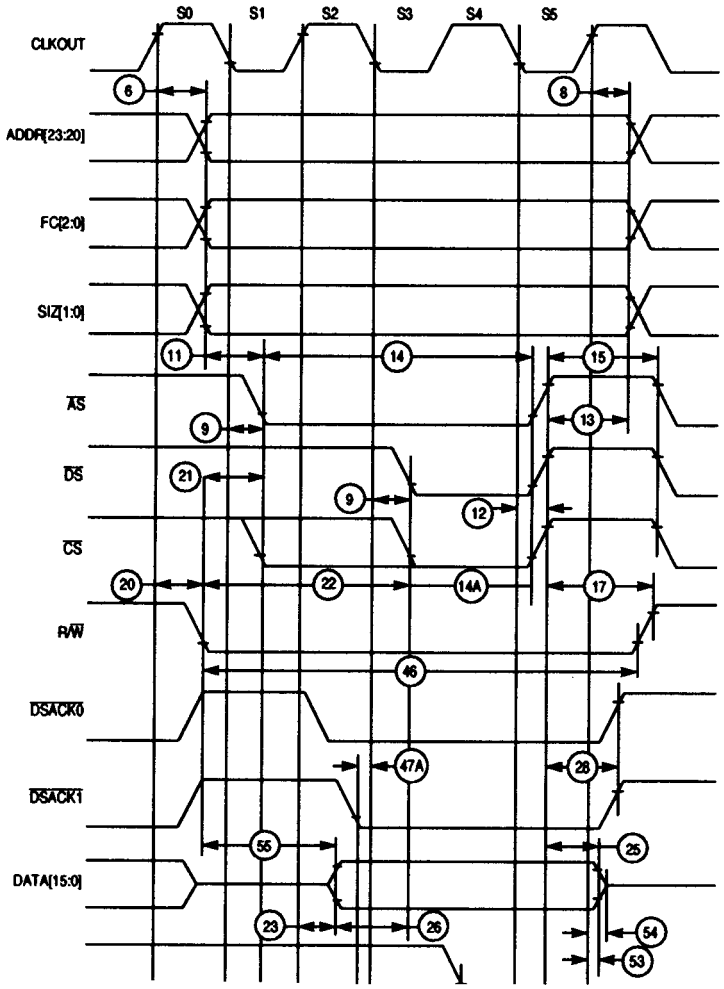
Question 3 (17 marks)

The diagram below shows part of the interface between a Motorola 68HC16 microprocessor and a Hyundai HY6264A SRAM:



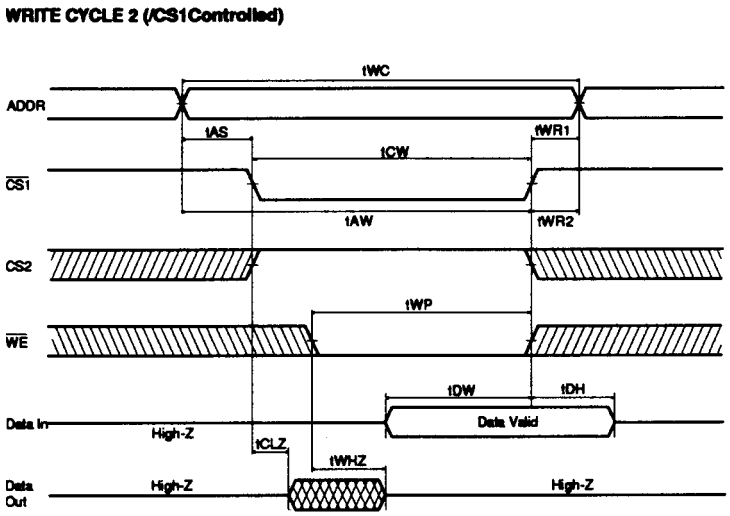
The microprocessor's data strobe (DS*) signal drives the RAM's chip select (CS1*). The RAM's write enable (WE*) is driven by the CPU's read/write signal (R/W*). The RAM's address and data buses are connected to the corresponding CPU buses.

The following timing diagram and table shows *some* of the CPU's write-cycle timing specifications. The clock (CLKOUT) period is 60ns and you may assume it is symmetrical (high for 30 ns and low for 30 ns). All times are in nanoseconds.



Number	Characteristic	Symbol	Min	Max
6	clock high to ADDR valid	t_{CHAV}	0	35
9	clock low to DS* asserted	t_{CLSA}	2	25
12	clock low to DS* negated	t_{CLSN}	2	29
13	DS* negated to ADDR invalid	t_{SNAI}	15	-
17	DS* negated to R/W* high	t_{SNRN}	15	-
23	clock high to data out valid	t_{CHDO}	-	30
25	DS* negated to data out invalid	t_{SNDOI}	15	-
46	R/W* width	t_{RWA}	150	-

The following diagram shows the SRAM write-cycle timing diagram.



The table below shows seven SRAM write-cycle timing requirements that need to be met. Obtain expressions for these requirements in terms of the symbols for the CPU timing specifications given above. Obtain values for these expressions in nanoseconds. Find the amount by which the requirement is exceeded (in nanoseconds) and state whether the requirement is met or not (Y[es] or N[o]). Give your answer in the form of a table as shown below (you may omit the first column).

Requirement			Guaranteed		Margin	Met
Parameter	Symbol	Min. (ns)	Expression	Value	(ns)	(Y/N)
Write Cycle Requirements						
Write Pulse Width	t_{WP}	50				
Data to Write Time Overlap	t_{DW}	35				
Data Hold from Write	t_{DH}	0				
Write Cycle	t_{WC}	70				
Chip Select to End of Write	t_{CW}	55				
Address Setup	t_{AS}	0				
Write Recovery	t_{WR2}	0				

Question 4 (8 marks)

You are designing a memory system for a CPU with a 32-bit data bus and a 24-bit address bus. Answer the following questions and show how you calculated your answers:

(a) How many bytes would be provided by using 32 chips each of which was “8k by 4”?

(b) What is the minimum number of "16k by 8" chips that could be used?

(c) How many "16k by 8" chips would be required to cover the address range from 00000H to 1FFFFH? How many banks of memory would there be?

(d) If the CPU uses byte addressing plus "byte enable" signals, how many address signals would be present on the CPU chip and how would they typically be labelled?

Question 5 (14 marks)

For the following questions you need not explain your answer. Make sure your answer is unambiguous.

(a) For each bus in column "A" select the best matching entry in column "B". Write your answers in numerical order and show the number and the selected letter unambiguously.

A		B	
1	PC-104	A	system bus
2	GPIB	B	bit stuffing
3	SCSI	C	data/address multiplexing
4	HDLC	D	BHE*/BLE*
5	PCI	E	talkers and listeners
6	386SX processor bus	E	peripheral bus

(b) Copy the following table into your exam book and fill in each entry with T (true) or F (false).

		open collector output	tri-state output
1	requires pull-up		
2	can source current		
3	can sink current		
4	uses output enable		

(c) Which of the following changes to the *transmission* format of ASCII characters over an RS-232 serial interface would not change the characters received?

1. Using two start bits?
2. Using two stop bits?

(d) On an IBM PC compatible computer, a timer signal asserts IRQ0 periodically so that the operating system can keep track of the time of day.

1. At what location is the address of the timer ISR stored?
2. Which of the following is the *minimum* number of things that need to be done before returning from the ISR (using `RTI`) to ensure that the timer ISR will run again:

(i) send the PIC an EOI instruction
(ii) set the IF bit
(iii) both (i) and (ii)
(iv) nothing