SPRS075A – OCTOBER 1998 – REVISED FEBRUARY 1999

- **Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus**
- **40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators**
- **17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation**
- **Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Data Bus With a Bus Holder Feature**
- **Extended Addressing Mode for 8M × 16-Bit Maximum Addressable External Program Space**
- **64K x 16-Bit On-Chip RAM Composed of:**
  - **Four Blocks of 2K × 16-Bit On-Chip Dual-Access Program/Data RAM**
  - **Seven Blocks of 8K × 16-Bit On-Chip Single-Access Program/Data RAM**
- **16K × 16-Bit On-Chip ROM Configured to Program Memory**
- **Enhanced External Parallel Interface (XIO2)**
- **Single-Instruction-Repeat and Block-Repeat Operations for Program Code**
- **Block-Memory-Move Instructions for Better Program and Data Management**
- **Instructions With a 32-Bit Long Word Operand**
- **Instructions With Two- or Three-Operand Reads**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
- **Fast Return From Interrupt**
- **On-Chip Peripherals**
  - **Software-Programmable Wait-State Generator and Programmable Bank-Switching**
  - **On-Chip Programmable Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source**
  - **One 16-Bit Timer**
  - **Six-Channel Direct Memory Access (DMA) Controller**
  - **Three Multichannel Buffered Serial Ports (McBSPs)**
  - **8-Bit Enhanced Parallel Host-Port Interface (HPI8)**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **CLKOUT Off Control to Disable CLKOUT**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **144-Pin Thin Quad Flatpack (TQFP) (PGE Suffix)**
- **176-Pin Ball Grid Array (BGA) (GGW Suffix)**
- **10-ns Single-Cycle Fixed-Point Instruction Execution Time (100 MIPS)**
- **3.3-V I/O Supply Voltage**
- **2.5-V Core Supply Voltage**

ADVANCE INFORMATION

description

The TMS320VC5410 fixed-point, digital signal processor (DSP) (hereafter referred to as the ’5410 unless otherwise specified) is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. This processor provides an arithmetic logic unit (ALU) with a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The basis of the operational flexibility and speed of this DSP is a highly specialized instruction set.

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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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terminal functions

The terminal functions table lists each signal, function, and operating mode(s) grouped by function.

Terminal Functions

TERMINAL NAME		I/O†	DESCRIPTION
DATA SIGNALS			
A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	(MSB) (LSB)	O/Z	Parallel address bus A22 [most significant bit (MSB)] through A0 [least significant bit (LSB)]. The sixteen LSB lines, A0 to A15, are multiplexed to address external memory (program, data) or I/O. The seven MSB lines, A16 to A22, address external program space memory. A22–A0 is placed in the high-impedance state in the hold mode. A22–A0 also goes into the high-impedance state when $\overline{OFF}$ is low. The address bus has a bus holder feature that eliminates passive components and the power dissipation associated with them. The bus holder keeps the address bus at the previous logic level when the bus goes into a high-impedance state.
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	(MSB) (LSB)	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). D15–D0 is multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. D15–D0 is placed in high-impedance state when not outputting data or when $\overline{RS}$ or $\overline{HOLD}$ is asserted. D15–D0 also goes into the high-impedance state when $\overline{OFF}$ is low. The data bus has a bus holder feature that eliminates passive components and the power dissipation associated with them. The bus holder keeps the data bus at the previous logic level when the bus goes into a high-impedance state. The bus holders on the data bus can be enabled/disabled under software control.

† I = Input, O = Output, Z = High-impedance, S = Supply

Terminal Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
INITIALIZATION, INTERRUPT AND RESET OPERATIONS		
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge signal. $\overline{\text{IACK}}$ indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–A0. $\overline{\text{IACK}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$	I	External user interrupt inputs. $\overline{\text{INT0}}$–$\overline{\text{INT3}}$ is prioritized and is maskable by the interrupt mask register (IMR) and interrupt mode bit. $\overline{\text{INT0}}$ –$\overline{\text{INT3}}$ can be polled and reset by way of the interrupt flag register (IFR).
$\overline{\text{NMI}}$	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is an external interrupt that cannot be masked by way of the INTM or the IMR. When $\overline{\text{NMI}}$ is activated, the processor traps to the appropriate vector location.
$\overline{\text{RS}}$	I	Reset. $\overline{\text{RS}}$ causes the digitial signal processor (DSP) to terminate execution and forces the program counter to 0FF80h. When $\overline{\text{RS}}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{\text{RS}}$ affects various registers and status bits.
MP/$\overline{\text{MC}}$	I	Microprocessor/microcomputer mode select pin. If active low at reset (microcomputer mode), MP/$\overline{\text{MC}}$ causes the internal program ROM to be mapped into the upper 16K words of program memory space. In the microprocessor mode, off-chip memory and its corresponding addresses (instead of internal program ROM) are accessed by the DSP.
MULTIPROCESSING SIGNALS		
$\overline{\text{BIO}}$	I	Branch control. A branch can be conditionally executed when $\overline{\text{BIO}}$ is active. If low, the processor executes the conditional instruction. The $\overline{\text{BIO}}$ condition is sampled during the decode phase of the pipeline for the XC instruction, and all other instructions sample $\overline{\text{BIO}}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or used as a general-purpose output pin. XF goes into the high-impedance state when $\overline{\text{OFF}}$ is low, and is set high at reset.
MEMORY CONTROL SIGNALS		
$\overline{\text{DS}}$ $\overline{\text{PS}}$ $\overline{\text{IS}}$	O/Z	Data, program, and I/O space select signals. $\overline{\text{DS}}$, $\overline{\text{PS}}$, and $\overline{\text{IS}}$ are always high unless driven low for communicating to a particular external space. Active period corresponds to valid address information. $\overline{\text{DS}}$, $\overline{\text{PS}}$, and $\overline{\text{IS}}$ are placed into the high-impedance state in the hold mode; these signals also go into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{MSTRB}}$	O/Z	Memory strobe signal. $\overline{\text{MSTRB}}$ is always high unless low-level asserted to indicate an external bus access to data or program memory. $\overline{\text{MSTRB}}$ is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
READY	I	Data ready. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{\text{W}}$	O/Z	Read/write signal. R/$\overline{\text{W}}$ indicates transfer direction during communication to an external device. R/$\overline{\text{W}}$ is normally in the read mode (high), unless it is asserted low when the DSP performs a write operation. R/$\overline{\text{W}}$ is placed in the high-impedance state in the hold mode; and it also goes into the high-impedance state when $\overline{\text{OFF}}$is low.
$\overline{\text{IOSTRB}}$	O/Z	I/O strobe signal. $\overline{\text{IOSTRB}}$ is always high unless low-level asserted to indicate an external bus access to an I/O device. $\overline{\text{IOSTRB}}$ is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{HOLD}}$	I	Hold input. $\overline{\text{HOLD}}$ is asserted to request control of the address, data, and control lines. When acknowledged by the 'VC5410, these lines go into the high-impedance state.
$\overline{\text{HOLDA}}$	O/Z	Hold acknowledge. $\overline{\text{HOLDA}}$ indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in the high-impedance state, allowing them to be available to the external circuitry. $\overline{\text{HOLDA}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{MSC}}$	O/Z	Microstate complete. $\overline{\text{MSC}}$ goes low when the last wait state of two or more internal software wait states programmed is executed. If connected to the READY line, $\overline{\text{MSC}}$ forces one external wait state after the last internal wait state has been completed. $\overline{\text{MSC}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.

† I = Input, O = Output, Z = High-impedance, S = Supply

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external multiply-by-N clock option

An external frequency source can be used by applying an input clock to X2/CLKIN with X1 left unconnected. Table 10 shows the configuration options for the CLKMD pins that generate the external divide-by-2 clock option. Following reset, the software PLL can be programmed for the desired multiplication factor. Refer to the *TMS320C54x DSP CPU and Peripherals Reference Set*, Volume 1 (literature number SPRU131) for detailed information on programming the PLL. The external input clock frequency is multiplied by the multiplication factor N to generate the internal CPU machine cycle.

The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 16 and the recommended operating conditions table)

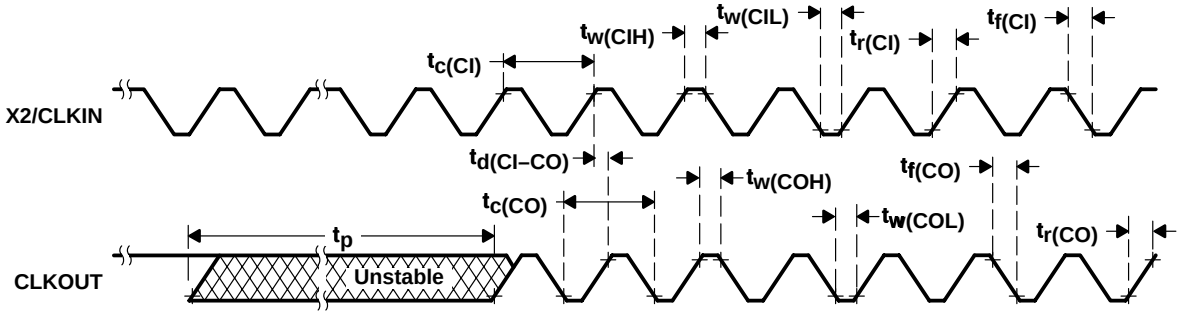
PARAMETER		’VC5410-100			UNIT
		MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT	10	$t_{c(CI)/N}$†		ns
$t_{d(CI-CO)}$	Delay time, X2/CLKIN high/low to CLKOUT high/low	3	6	10	ns
$t_{f(CO)}$	Fall time, CLKOUT		2		ns
$t_{r(CO)}$	Rise time, CLKOUT		2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H–2	H–1	H	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H–2	H–1	H	ns
t_p	Transitory phase, PLL lock-up time			35	µs

† N is the multiplication factor.

timing requirements† (see Figure 16)

			’VC5410-100		UNIT
			MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	Integer PLL multiplier N (N = 1–15)	10N	400N	ns
		PLL multiplier N = x.5	10N	200N	
		PLL multiplier N = x.25, x.75	10N	100N	
$t_{f(CI)}$	Fall time, X2/CLKIN			2	ns
$t_{r(CI)}$	Rise time, X2/CLKIN			2	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low		2		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high		2		ns

† N is the multiplication factor.



NOTE A: The CLKOUT timing in this diagram assumes the CLKOUT divide factor (DIVFCT field in the BSCR) is configured as 00 (CLKOUT not divided). DIVFCT is configured as CLKOUT divided-by-4 mode following reset.

Figure 16. External Multiply-by-One Clock Timing

memory and parallel I/O interface timing

memory read

External memory reads can be performed in consecutive or nonconsecutive mode under control of the CONSEC bit in the BSCR.

switching characteristics over recommended operating conditions ($\overline{\text{MSTRB}}$ = 0) † (see Figure 17 and Figure 18)

PARAMETER		'VC5410-100		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid	– 1	4	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low	– 1	4	ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high	– 1	4	ns

† Address,R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

timing requirements ($\overline{\text{MSTRB}}$ = 0) [H = 0.5 $t_{c(CO)}$]† (see Figure 17 and Figure 18)

		'VC5410-100		UNIT
		MIN	MAX	
$t_{a(A)M1}$	Access time, read data access from address valid, first read access		4H–8	ns
$t_{a(A)M2}$	Access time, read data access from address valid, consecutive read accesses		2H–8	ns
$t_{su(D)R}$	Setup time, read data valid before CLKOUT low	5		ns
$t_{h(D)R}$	Hold time, read data valid after CLKOUT low	0		ns

† Address,R/$\overline{W}$, $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ timings are all included in timings referenced as address.

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memory and parallel I/O interface timing (continued)

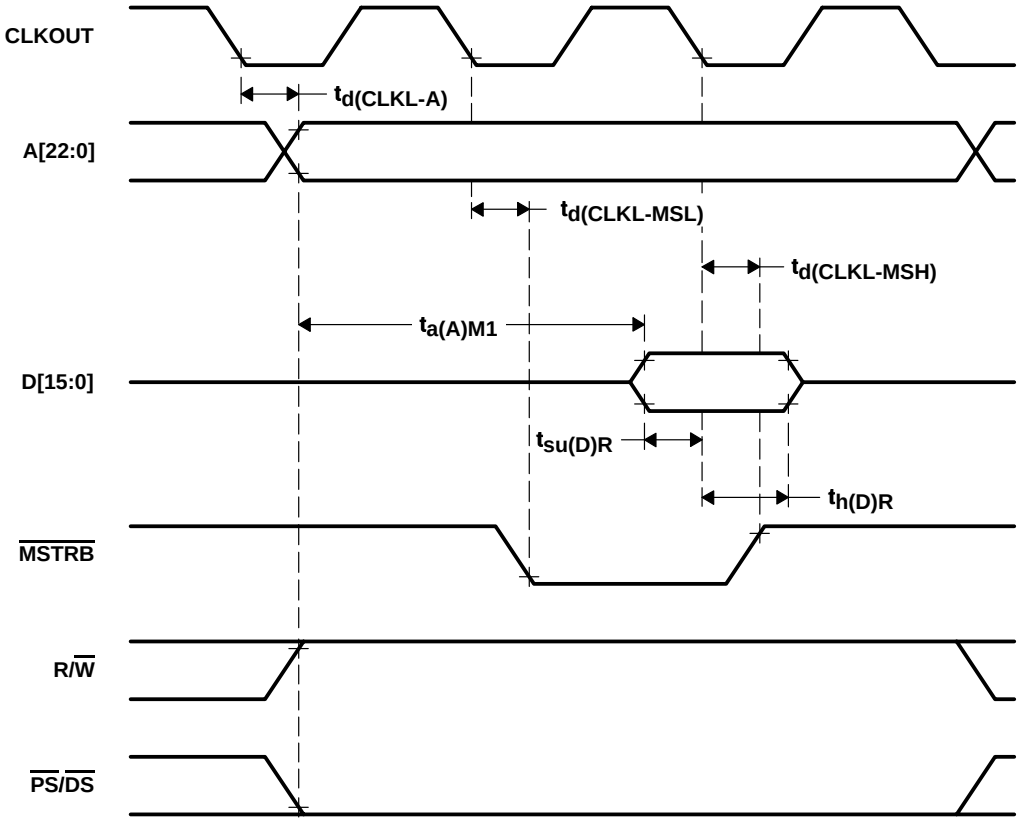

Figure 17. Nonconsecutive Mode Memory Reads

ADVANCE INFORMATION

memory and parallel I/O interface timing (continued)

memory write

switching characteristics over recommended operating conditions ($\overline{\text{MSTRB}}$ = 0) [H = 0.5 $t_{c(CO)}$]† (see Figure 19)

PARAMETER		’VC5410-100		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, CLKOUT low to address valid	– 1	4	ns
$t_{su(A)MSL}$	Setup time, address valid before $\overline{\text{MSTRB}}$ low	2H – 5		ns
$t_{d(CLKL-D)W}$	Delay time, CLKOUT low to data valid	– 1	4	ns
$t_{su(D)MSH}$	Setup time, data valid before $\overline{\text{MSTRB}}$ high	2H – 5	2H + 5	ns
$t_{h(D)MSH}$	Hold time, data valid after $\overline{\text{MSTRB}}$ high	2H – 5	2H + 5	ns
$t_{d(CLKL-MSL)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low	– 1	4	ns
$t_{w(SL)MS}$	Pulse duration, $\overline{\text{MSTRB}}$ low	2H – 5		ns
$t_{d(CLKL-MSH)}$	Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high	– 1	4	ns

† Address, R/$\overline{\text{W}}$, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{IS}}$ timings are all included in timings referenced as address.

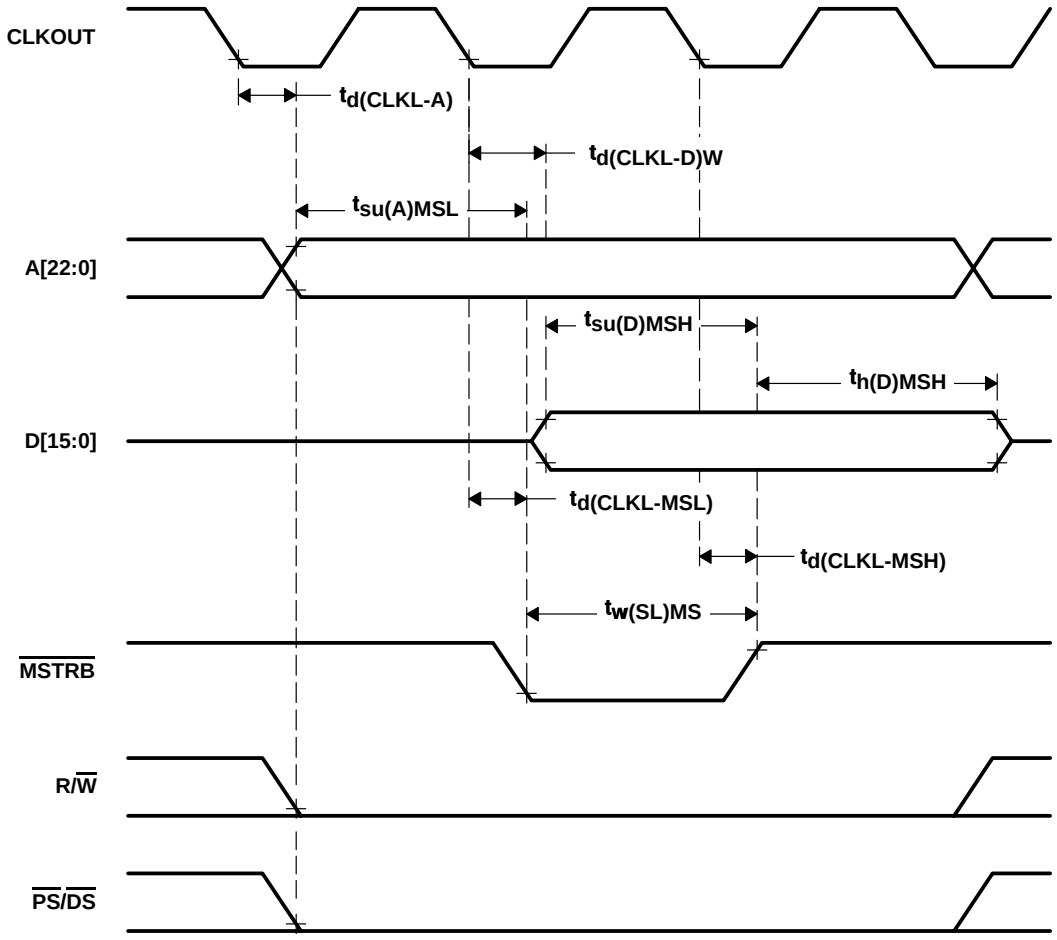

Figure 19. Memory Write ($\overline{\text{MSTRB}}$ = 0)