Solution to Assignment 5
Timing Analysis

Question 1

$H = 5$ns. All times in nanoseconds. Note that if the margin is zero the specification is met.

Timing Requirements

CPU Read Cycle

$t_{a(A)M1}$	$4H-8=12$
$t_{su(D)R}$	5
$t_{h(D)R}$	0

CPU Write Cycle

No timing requirements.

RAM Read Cycle

t_{RC}	10

RAM Write Cycle

The circuit shown in the assignment is incorrect because a write cycle could only be terminated by either DS* (CS*) or R/W* (WE*) going high. Consecutive write cycles therefore would not terminate. The following analysis assumes that the write cycle will be terminated by either DS* or R/W* going high (write cycle 3 or 2 respectively).

t_{WC}	10
t_{CW}	7
t_{AS}	0
t_{AW}	7
t_{WP1}	10
t_{BW}	7
t_{WR}	0
t_{DW}	5
t_{DH}	0

Flash Read Cycle

No timing requirements.

Timing Analysis

CPU Requirements - RAM Read Cycle

	req'd	expression	margin
$t_{a(A)M1}$	12	t_{AA} or $t_{CO}=10$	2
$t_{su(D)R}$	5	$4H-t_{d(CLKL-A)}-t_{AA}=$ $20-4-10=6$	1
$t_{h(D)R}$	0	$t_{OH}+t_{d(CLKL-A)}=$ $3+-1=2$	2

CPU Requirements - Flash Read Cycle

	req'd	expression	margin
$t_{a(A)M1}$	12	t_{ACC} or $t_{CE}=55$	-43
$t_{su(D)R}$	5	$4H-t_{d(CLKL-A)}-t_{ACC}=$ $20-4-55=-39$	-44
$t_{h(D)R}$	0	$t_{OH}+t_{d(CLKL-A)}$ $0+-1=-1$	-1

For the first two requirements an additional 5 wait states (50 ns) would be required to meet the requirements. The hold time requirement cannot be met by adding wait states.

RAM Requirements - CPU Read Cycle

	req'd	expression	margin
t_{RC}	10	$4H=20$	10

RAM Requirements - CPU Write Cycle

	req'd	expression	margin
t_{WC}	10	$4H = 20$	10
t_{CW}	7	$4H = 20$	13
t_{AS}	0	?	?
t_{AW}	7	$4H = 20$	13
t_{WP1}	10	$4H = 20$	10
t_{BW}	7	—	—
t_{WR}	0	?	?
t_{DW}	5	$2H - t_{d(CLKL\text{-}D)W} + t_{d(CLKL\text{-}A)} = 10 - 4 - 1 = 5$	0
t_{DH}	0	$t_{d(CLKL\text{-}MSH)} + t_{h(D)MSH} + t_{d(CLKL\text{-}A)} = -1 + 5 + -1 = 3$	3

When evaluating the guaranteed cycle time (t_{WC}) and pulse widths on R/W* and DS* (t_{CW} and t_{WP1}) I have assumed that the timing delays will be constant from bus cycle to bus cycle (i.e. that each bus cycle is exactly 4H long). If you did not make this assumption then the pulse widths would be 5 ns smaller (max to min range of $t_{d(CLKL\text{-}A)}$).

The CPU address setup time (t_{AS}) and write recovery time (t_{WR}) are not specified, and it would be wrong to assume a value of 0 simply by looking at the timing diagram.

Since UB* and LB* are tied low, the t_{BW} duration requirements will always be met.

The data hold time can only be obtained indirectly by looking at the timing of the MSTRB signal. This sort of indirect analysis isn't always valid.