Solution to Assignment 1
VHDL Synthesis

Question 1

```
entity ec74ls168 is
port (
   ud, pe, cet, cep, cp : in bit ;
   p : in bit_vector (3 downto 0) ;
   q : out bit_vector (3 downto 0) ;
   tc : out bit ) ;
end ec74ls168 ;

architecture rtl of ec74ls168 is
   signal count, next_count,
      up_count, down_count : bit_vector (3 downto 0) ;
   signal operation : bit_vector (2 downto 0) ;
   signal tc_selector : bit_vector (5 downto 0) ;
   signal countenable : bit ;
begin

with count select up_count <=
   "0001" when "0000",
   "0010" when "0001",
   "0011" when "0010",
   "0100" when "0011",
   "0101" when "0100",
   "0110" when "0101",
   "0111" when "0110",
   "1000" when "0111",
   "1001" when "1000",
   "0000" when "1001",
   "1011" when "1010",
   "0100" when "1011",
   "1101" when "1100",
   "0100" when "1101",
   "1111" when "1110",
   "0000" when others ;

with count select down_count <=
   "0000" when "0001",
   "0001" when "0010",
   "0010" when "0011",
   "0011" when "0100",
   "0100" when "0101",
   "0101" when "0110",
   "0110" when "0111",
   "0111" when "1000",
   "0000" when "1001",
   "0001" when "1010",
   "1010" when "1011",
   "0011" when "1100",
   "1100" when "1101",
   "0101" when "1110",
   "1110" when others ;

countenable <= ( not cet ) and ( not cep ) ;

operation <= pe & countenable & ud ;

with operation select next_count <=
   p          when "000",
   p          when "001",
   p          when "010",
   p          when "011",
   count      when "100",
   count      when "101",
   down_count when "110",
   up_count   when "111" ;

process(cp)
begin
   if cp'event and cp = '1' then
      count <= next_count ;
   end if ;
end process ;

q <= count ;

tc_selector <= cet & ud & count ;

with tc_selector select tc <=
   '1' when "011001", --  9
   '1' when "011011", -- 11
   '1' when "011101", -- 13
   '1' when "011111", -- 15
   '1' when "000000", -- down
   '0' when others ;

end rtl ;
```

Figure 1 shows the simulation results.

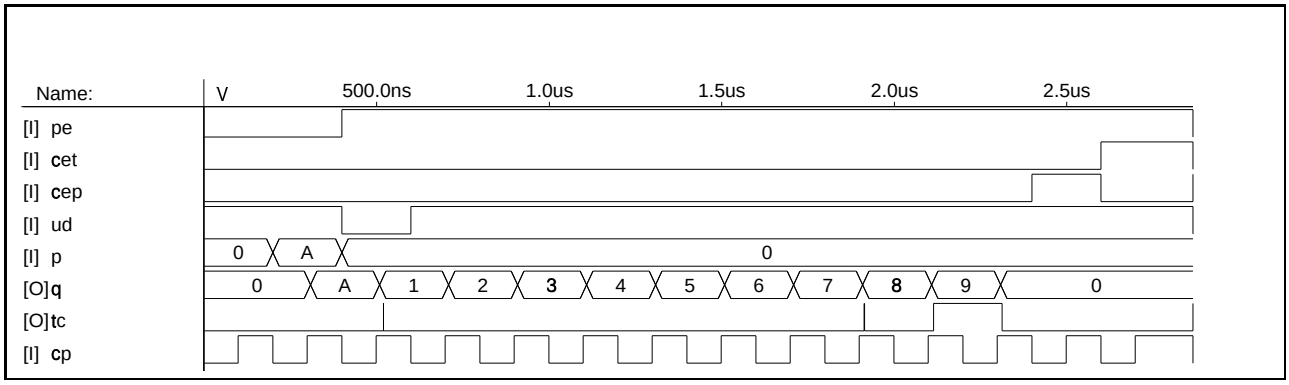

Figure 1: Simulation Results.