ELEC 379 : DESIGN OF DIGITAL AND MICROCOMPUTER SYSTEMS
1998/99 WINTER SESSION, TERM 2

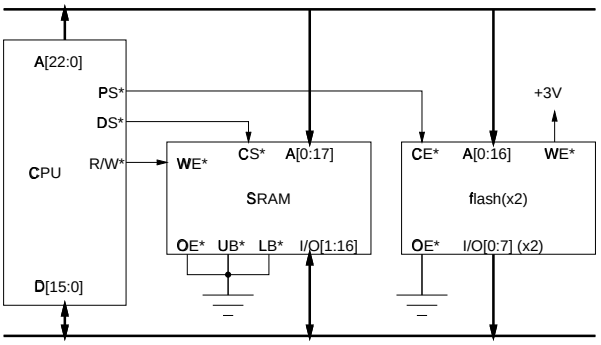
Assignment 5 - Timing Analysis

due
Wednesday, March 31 1999

There was no assignment titled "Assignment 4." Instead the second part of Assignment 3 will be counted as Assignment 4.

Question 1

This assignment asks you to analyze the timing requirements for the CPU and memory devices in a small microcomputer system. The design consists of: (1) a TI TMS320C5410 microprocessor operating at 100 MHz, (2) a Samsung KM616V4002BL-10 256k $\times$ 16 SRAM, and (3) two Atmel AT49HLV010-55 128k $\times$ 8 'flash' EEPROMs connected as shown below:



Links to the manufacturer's data sheets for these devices are available on the course Web page. To do this assignment you'll only need to print out the pages containing the signal definitions, timing specifications and timing diagrams from each data sheet.

The CPU clock frequency is 100 MHz (H=5ns) and it is configured to performs non-consecutive mode memory reads only.

Read bus cycles (Figure 17) take two clock cycles. The CPU puts the address on the data bus and asserts PS* or DS* during the first clock cycle. The CPU then latches the data at the end of this second cycle.

Write bus cycles (Figure 19) also take two clock cycles. The CPU puts the address on the data bus and asserts PS* or DS* during the first cycle. The CPU puts the data on the data bus during both the second clock cycle of the write cycle and the first clock cycle of the subsequent bus cycle.

In this design the flash is read-only. The SRAM is enabled by the DS* (data space) and the flash is enabled by PS* (program space) signals from the CPU. The SRAM write enable (WE*) is controlled by the CPU's R/W* signal.

From your understanding of CPU bus cycles prepare a list of each CPU memory (not i/o) read and write cycle timing requirement (p. 43 and 46). Repeat for the RAM read and write cycle specifications (p. 4 and 5) and for the flash read cycle specifications (p. 5). Include in your list only the timing requirements, not the guaranteed responses.

Perform a timing analysis for three types of cycles: RAM read, RAM write and flash read (word). For each cycle, obtain an *equation* for each timing requirement as a function of the guaranteed responses and the clock period and then compute the margin available for each requirement (negative if the requirement is not met). For each requirement that is not met, find the number of additional wait states (clock periods) that would have to be inserted so that the requirement would be met. Note any requirements where it is not possible to determine if the requirements are met.

A more detailed timing analysis would also consider consecutive read and write cycles to ensure that bus conflicts did not occurr. You need not do this for this assignment.

Your answer should include the list of all of the timing requirements and one table for each combination of device and bus cycle that has timing requirements.