Assignment 1 - VHDL Synthesis

due Wednesday, January 27, 1999

Question 1

In this assignment you'll write a VHDL circuit description and synthesize it into a schematic.

Retrieve the 6-page data sheet for the 74LS168 4-bit decade counter in PDF format from the Motorola Web site (the URL is given on the course Web page). Print the first four pages.

Write a VHDL entity statement for this device. Use the same signal names (e.g. `ud`, `cep`, etc) as used in the data sheet. Use `bit_vector` types with indices (`(3 downto 0)`) as appropriate. Ignore power (Vcc) and ground. Use your initials plus the digits 168 as the entity name (e.g. if your name is Doug Mah, your entity statement would begin "`entity DM168 is` ...").

Write an architecture that models the behaviour of the device. Assume positive true logic (0 = L, 1 = H). Don't worry if your description ends up looking rather long-winded.

Include comments giving at least the purpose of the circuit, your name and student number, the course and the date.

Synthesize your design using MaxPlusII and simulate its operation showing that the device correctly performs the following sequence of operations (number of clock cycles shown in parentheses):

- loads 0 (1)
- loads 10 (1)
- counts down from 10 to 1 (9)
- counts up from 1 to 9 and "wraps around" back to 0 (9)
- output does not change up when CET* is not asserted (1)
- output does not change up when CEP* is not asserted (1)

Hand in a listing of your VHDL code and the simulation results.