Solutions to Assignment 5

Question 1

There are three cycles to be analyzed: SRAM write, SRAM read and EPROM read. In each case the device into which the data is being latched (the SRAM, the CPU and the CPU respectively) is the device whose timing requirements have to be met. The specifications which are timing requirements are those that specify a clock edge on the chip into which data is being loaded.

The following sections give the timing requirements for each of the devices. For each requirement the following are given: the symbol, a description of the requirement, the required minimum or maximum value, an expression for the guaranteed value, and the margin. All numerical values are in nanoseconds.

SRAM Write Cycle (from 8051 CPU)

t_{WC}
address valid to address valid
minimum of 85 ns
The guaranteed minimum cycle period is not given, however, it will be longer than $t_{AVWL} + t_{WLWH} + t_{WHQX}$ = 203+400+33=636 ns so the requirement will certainly be met (other bounds are also possible). Other 8051 data sheets state that the external memory write cycle takes 12 clock cycles or 1000 ns.

t_{CW}
chip select to w*/cs* high
minimum of 70
$= t_{AVWL} + t_{WLWH}$
= 203+400 = 603 ns
met by 533 ns

t_{AW}
address valid to w*/cs* high
minimum of 70 ns
margin is same as above

t_{WP}
write low to write high
minimum of 60 ns
$= t_{WLWH}$ = 400 ns
met by 340 ns

t_{DW}
data valid to w*/cs* high
minimum of 35 ns
$= t_{QVWX} + t_{WLWH}$ = 23 + 400 = 423
met by 388 ns

t_{DH}
w*/cs* high to data invalid
minimum of 0 ns
$= t_{WHQX}$ = 33 ns
met by 33 ns

t_{AS}
address valid to write low
minimum of 0 ns
$= t_{AVWL}$ = 203 ns
met by 203 ns

t_{WR}
write high to address invalid
minimum of 0 ns
This is not given, however it will be greater than t_{WHQX} = 33 ns since the address cannot appear on Port 0 and Port 2 until the data is removed.
met by at least 33 ns

Intel 8051 Program Memory Read Cycle (from EPROM)

t_{LLIV}
latch low to instruction valid
maximum of 224 ns

guaranteed value not given and not possible to determine.

t_{PLIV}
PSEN* low to instruction valid
maximum of 135 ns
= ten(G) = 100 ns
met by 35 ns

t_{PXIX}
PSEN* high to instruction invalid
minimum of 0 ns
= t_v(A) = 0 ns
met by 0 ns

t_{PXIZ}
PSEN* high to instruction float
maximum of 59 ns
t_{dis} = 60 ns max
not met by 1 ns
For clock frequencies other than 12 MHz the requirement is t_{PXIZ} = t_{CLCL} - 25 = 60 ns. The maximum clock period is thus (60 + 25) = 85 ns and the maximum clock frequency = 1/85 ns = 11.8 MHz.

t_{AVIV}
address valid to instruction valid
maximum of 312 ns
= t_a(A) = 250 ns
met by 62 ns

Intel 8051 Data Memory Read Cycle (from SRAM)

t_{RLDV}
read low to data valid
maximum of 252 ns
= t_{OE} = 40 ns
met by 212 ns

t_{RHDX}
read high to data invalid
minimum of 0 ns
guaranteed value not given (the specification t_{OHZ} is to data float, not to data invalid).

t_{RHDZ}
read high to data float
maximum of 97 ns
t_{OHZ} = 30 ns
met by 67 ns

t_{LLDV}
latch low to data valid
maximum of 517 ns
guaranteed value not given

t_{AVDV}
address valid to data valid
maximum of 585 ns
t_{AA} = 85 ns
met by 500 ns