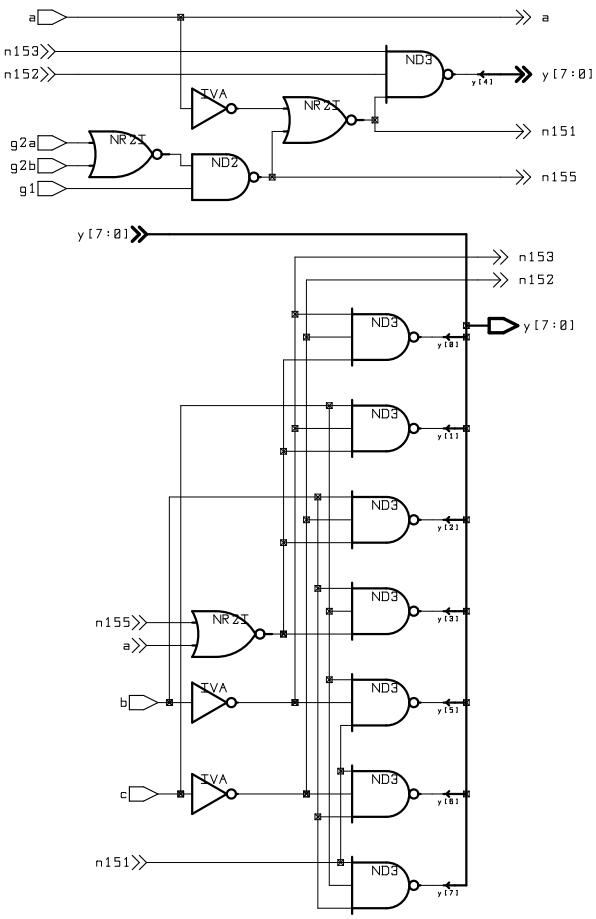
Solution to Assignment 1

Question 1

A possible solution is shown below. An if/else statement is used to model the output enables and a case statement is used to set the outputs.

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-- ELEC 379 Assignment 1 Solution
-- 74HCA138 3-to-8 decoder
-- Ed Casas, Jan 16 1998


entity MM74HCA138 is port (
   a, b, c : in bit ;
   g1, g2a, g2b : in bit ;
   y : out bit_vector (7 downto 0) ) ;
end MM74HCA138 ;


architecture rtl of MM74HCA138 is
   signal tmp : bit_vector (2 downto 0) ;
begin

   -- build vector so can use case statment
   process(a,b,c)
   begin
      tmp <= a & b & c ;
   end process ;

   process(tmp,g1,g2a,g2b)
   begin
      if g1 = '1' and g2a = '0' and g2b = '0'
      then
         case tmp is
         when "000" => y <= "11111110" ;
         when "001" => y <= "11111101" ;
         when "010" => y <= "11111011" ;
         when "011" => y <= "11110111" ;
         when "100" => y <= "11101111" ;
         when "101" => y <= "11011111" ;
         when "110" => y <= "10111111" ;
         when "111" => y <= "01111111" ;
         end case ;
      else
         y <= "11111111" ;
      end if ;
   end process ;

end rtl ;
```

The resulting schematic is: