Solutions to Mid-Term Exam

Question 1

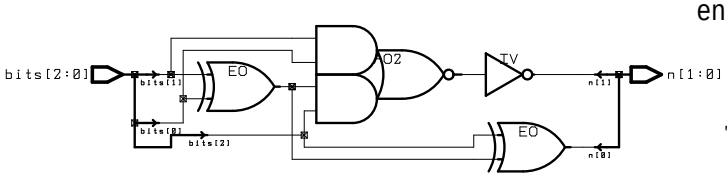
(a) The truth table is:

inputs			outputs	
a_2	a_1	a_0	n_1	n_0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(b) There are many possible solutions. A simple one is:

```
architecture rtl of nbits is
begin
   with bits select n <=
      "00" when "000",
      "01" when "001",
      "01" when "010",
      "10" when "011",
      "01" when "100",
      "10" when "101",
      "10" when "110",
      "11" when "111" ;
end rtl ;
```

The resulting schematic is:

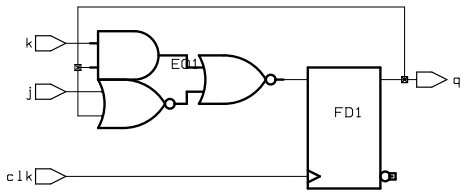


Question 2

Many solutions are possible. The following solution separates the combination and sequential parts of the design (this is always a good idea). It is necessary to use an internal copy of the output (`iq`) because VHDL does not allow outputs (in this case the flip-flop state, `q`) cannot be read.

```
architecture rtl of jkff is
   signal nq : std_logic ; -- next  q
   signal iq : std_logic ; -- internal q
begin

   -- combinational logic
   nq <=
      iq  when j = '0' and k = '0' else
      '0' when j = '0' and k = '1' else
      '1' when j = '1' and k = '0' else
      '1' when j = '1' and k = '1' and
         iq = '0' else
      '0' ; -- when j = '1' and k = '1' and
            -- iq = '1' ;

   -- sequential logic
   process(clk)
   begin
      if clk'event and clk='1' then
         iq <= nq ;
      end if ;
   end process ;

   -- outputs
   q <= iq ;

end rtl ;
```

The resulting schematic is:



Question 3

1. *chips per bank*: To create an 8-bit wide data bus using 4-bit chips we need $8/4 = 2$ chips per bank.

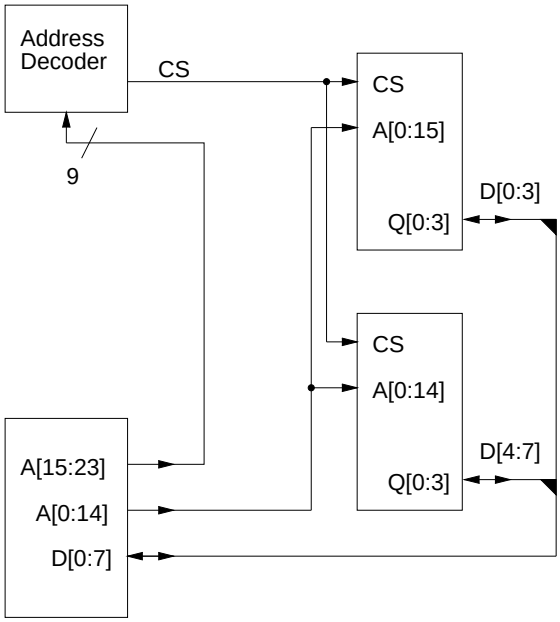
2. *number of banks*: Each bank provides 32 k words of 1 byte/word for a total of 32 k bytes per bank. With 2 chips we can provide $32\text{k}/32\text{k} = 1$ banks.

3. *byte-select address lines*: To select from the 1 bytes available in parallel we need to use the $\log_2 1 = 0$ least-significant CPU address bits.

4. *word-select address lines:* To select one word in each bank we need $\log_2 32\text{k} = 15$ address bus bits (A0 to A14).

5. *bank-select address lines:* The remaining $(24 - 15 = 9)$ address lines (A15 to A23) are then used to select a bank.

(a) The schematic of the memory system is as follows:



(b) The binary representation of the starting address, 220000 (hex), is 0010 0010 0000 0000 0000 0000. Since the memory requires 15 bits the address bit patterns that the memory will respond to is 0010 0010 0*XXX XXXX XXXX XXXX*.