THE UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ELEC 379 : Microcomputer System Design
1997/98 Winter Session Term 2

MID-TERM EXAMINATION
8:30 am – 9:20 am
February 27, 1997

This exam has three (3) questions. The marks for each question are as indicated. There are a total of 30 marks. Answer all questions. Write your answers in the exam book provided. Show your work. You may answer the questions in any order. Books, notes and calculators are allowed. You may keep this exam paper.

Question 1 (10 marks)

Design a "ones-counter" logic device that counts the number of bits that are set to '1' in a 3-bit input word. The device should have a three-bit input and a two-bit output. If the output is viewed as a binary number then its value should be the number of bits in the input that are set to '1'. For example, if the input is "010" then the output should be "01" (1), if the input is "111" the output should be "11" (3), if the input is "000" the output should be "00" (0), etc.

(a) Write out the truth table for this device.

(b) Given the following VHDL entity, write an architecture that implements this device. Your design should be synthesizeable by Synopsys Design Compiler.

```
entity nbits is
   port (
      bits : in bit_vector (2 downto 0) ;
      n : out bit_vector (1 downto 0) ) ;
end nbits ;
```

You need not include comments, `library` or `use` statements.

Question 2 (8 marks)

This question asks you to write a VHDL description for a JK flip-flop. This device has two inputs (`J` and `K`), a clock (`clk`), and one output (`Q`).

The output changes only on the rising edge of the clock. If both inputs are '0' then the output does not change; if only `J` is '1' the output is set to '1'; if only `K` is '1' the output is set to '0' and if `J` and `K` are both '1' then the value of the output is flipped ('0' to '1' or '1' to '0').

Given the following VHDL entity, write an architecture that implements this device. Your design should be synthesizeable by Synopsys Design Compiler.

```
entity jkff is
   port (
      j, k, clk : in std_logic ;
      q : out std_logic ) ;
end jkff ;
```

You need not include comments, `library` or `use` statements.

Question 3 (11 marks)

Draw the schematic of a memory system for an 8-bit CPU using two 32k by 4 ROMs. Assume the CPU has a 24-bit address bus (`A0` to `A23`), an 8-bit data bus (`D0` to `D7`). Each memory chip has data out pins (`Q0` to `Q3`), address inputs (`A0`, `A1`, ...), an active-low chip-select signal (`CS*`). The `CS*` pins should be driven from an address decoding circuit. You may assume all memory chips' outputs are tri-stated when the `CS*` is not asserted.

(a) Show the connections between the CPU, the decoder and the memory chip pins. The connections must be unambiguous. You may use the bus notation described in Assignment 4. The details of the address decoder need not be shown.

(b) The decoder is designed to place the RAM starting at location 220000 (hex). Show the address bit patterns that the memory will respond to (use '1', '0' and 'X').