THE UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ELEC 379 : Microcomputer System Design
1997/98 Winter Session Term 2

FINAL EXAMINATION
12:00 PM – 3:00 PM
April 29, 1998

This exam has five (5) questions. The marks for each question are as indicated. There are a total of 50 marks. Answer all questions. Write your answers in the exam book provided. Show your work. You may answer the questions in any order. Books, notes and calculators are allowed. You may keep this exam paper.

Question 1 (10 marks)

Write a synthesizeable VHDL description of a "presetable 4-bit binary counter" that meets the following specifications. The device has the following VHDL entity declaration:

```
library ieee ;
use ieee.std_logic_1164.all ;
use ieee.std_logic_arith.all ;

entity p4bc is
   port (
      clk, enable, load : in std_logic ;
      d : in unsigned (3 downto 0) ;
      q : out unsigned (3 downto 0) ) ;
end p4bc ;
```

The only output, `q`, is a 4-bit binary number (`q(3)` being the MS bit). The device is synchronous – the output can only change on the rising edge of the clock, `clk`. If `load` is '1' the values on the `d` inputs are copied to `q`. If `load` is '0' and `enable` is '1', the value of `q` is incremented. Otherwise the value of `q` does not change.

Write an architecture that implements this device. Your design should be synthesizeable by Synopsys Design Compiler. You need not include comments, `library` or `use` statements.

Hint: use "+"

Question 2 (10 marks)

Write a synthesizeable VHDL description of a "wait state generator" (a device which forces a CPU to execute wait states) that meets the following specifications. The device has the following VHDL entity declaration:

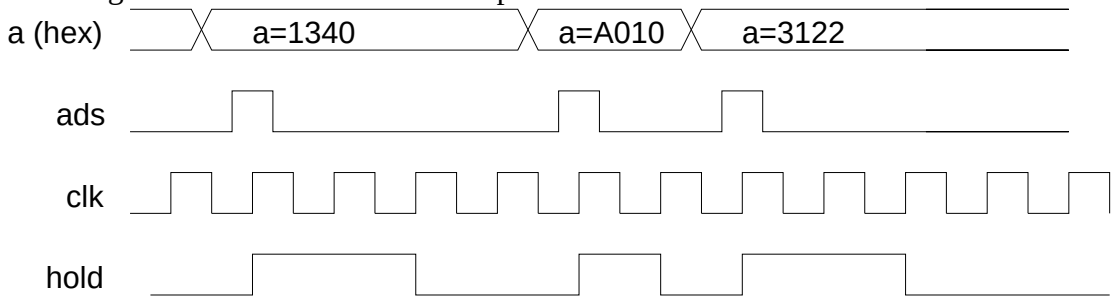
```
library ieee ;
use ieee.std_logic_1164.all ;

entity wsg is
   port (
      clk, ads : in std_logic ;
      a : in std_logic_vector (15 downto 0) ;
      hold : out std_logic ) ;
end wsg ;
```

The device has three inputs: a 16-bit address from the CPU (`a`), an active-high address strobe from the CPU (`ads`) which is active to indicate the start of a CPU cycle and a clock (`clk`).

The device has one output, an active-high signal (`hold`) that indicates to the CPU that the CPU cycle is not yet complete.

Normally `hold` is not asserted. If `ads` is asserted on the rising edge of the clock then your circuit should assert the `hold` output for a number of clock cycles that depends on the address: if the address is in the range 8000 to FFFF (hex) then `hold` should be asserted for one clock cycle; for other addresses `hold` should be asserted for two clock cycles.

The diagram below shows some examples:

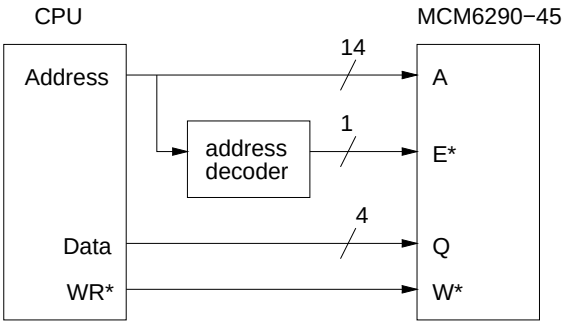


Write an architecture that implements this device. Your design should be synthesizeable by Synopsys Design Compiler. You need not include comments, `library` or `use` statements.

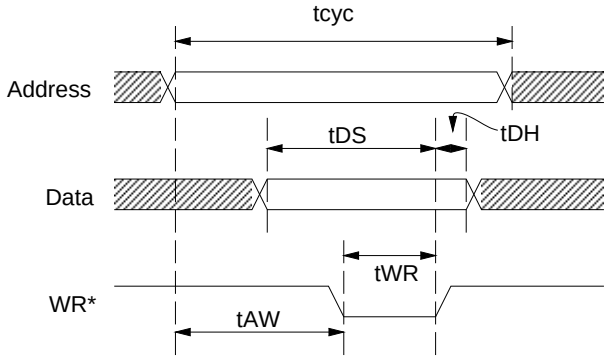
Hints: The MS bit of the address (a(15)) is sufficient to determine the address range. To help in your design you may want to draw the device states on the above timing diagram.

Question 3 (10 marks)

The diagram below shows part of the interface between a hypothetical microprocessor and a Motorola MC6290-45 static RAM. An address decoder drives the RAM's chip enable (E*). The RAM's write enable (W*) is driven by the CPU's write strobe (WR*). The RAM's address and data buses are driven by the corresponding CPU buses.

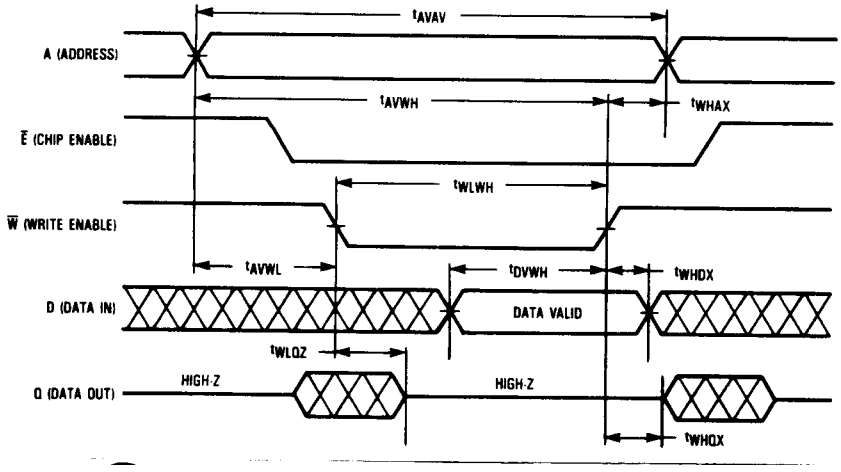


The following timing diagram and table gives the CPU's write-cycle timing specifications. Read-cycle timing specifications have been omitted.



Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	100	100	ns
Data Setup	t_{DS}	25	-	ns
Data Hold	t_{DH}	0	-	ns
Write Width	t_{WR}	33	-	ns
Write Delay	t_{AW}	40	-	ns

The following timing diagram shows the SRAM write-cycle timing diagram.



The table below shows six SRAM write-cycle timing requirements that need to be met. Obtain expressions for these requirements in terms of the symbols for the CPU timing specifications given above. Obtain values for these expressions in nanoseconds. Find the amount by which the requirement is exceeded (in nanoseconds) and state whether the requirement is met or not (Y[es] or N[o]). Give your answer in the form of a table as shown below (you may omit the first column).

Requirement			Guaranteed		Margin	Met
Parameter	Symbol	Min. (ns)	Expression	Value	(ns)	(Y/N)
Write Cycle Requirements						
Write Cycle	t_{AVAV}	45				
Address Setup	t_{AVWL}	0				
Address Valid to End of Write	t_{AVWH}	35				
Write Pulse Width	t_{WLWH}	35				
Data Valid to End of Write	t_{DVWH}	20				
Data Hold	t_{WHDX}	0				

Question 4 (10 marks)

Draw the schematic of a memory system for a 16-bit CPU providing a total of 64 kBytes using 16k by 4 ROMs. Assume the CPU has a 20-bit address bus (of which `A1` to `A23` are available externally), and a 16-bit data bus (`D0` to `D15`). Each memory chip has data out pins (`Q0`, `Q1`, ...), address inputs (`A0`, `A1`, ...), and an active-low chip-select signal (`CS*`). The `CS*` pins should be driven from an address decoding circuit with an appropriate number of outputs. You may assume all memory chips' outputs are tri-stated when the `CS*` is not asserted.

Show the connections between the CPU, the decoder and the memory chip pins. The connections must be *unambiguous*. You may use the bus notation described in Assignment 4. The details of the address decoder need not be shown.

Hint: Use a full page to draw your diagram.

Question 5 (10 marks)

For the following questions you need not explain your answer. Make sure your answer is unambiguous.

(a) Which of the following timing specifications would you expect a ROM to have: (i) a hold time, (ii) a setup time, (iii) an access time? Which of these specifications would you expect a DRAM to have?

(b) For each type of memory in column "A" select the best matching entry in column "B". Write your answers in numerical order and show the number and the selected letter unambiguously.

A		B	
1	DRAM	A	8 kB data memory in fast DSP processor
2	SRAM	B	software-upgradeable boot-up code in a PC
3	flash EEPROM	C	program memory for a video game cartridge
4	OTP ROM	D	8 MB image buffer in laser printer

(c) The value 3456 (hex) is written to memory location 2001 (hex) by an Intel 386SX processor. Which memory location(s) will be written (specify the byte the address(es))? What will the new value(s) be?

(d) On an IBM PC compatible computer the ISR for the first serial port (connected to the PIC's IR4 input) was executing when the timer caused the PIC's IR0 input to be asserted. What are the minimum steps that must have happened so that the timer ISR will be executed:

(i) the serial port ISR sent the PIC an EOI instruction

(ii) the serial port ISR set the IF bit

(iii) both (i) and (ii)

(e) The RTS/CTS pins are used by the standard (original) RS-232 interface to control the flow of data:

(i) from the DCE to the DTE

(ii) from the DTE to the DCE

(iii) both (i) and (ii)