Assignment 5 - Timing Analysis

Due Friday, March 13, 1998

In this assignment you will perform a complete timing analysis on a simple but realistic microcomputer system.

1 Question 1

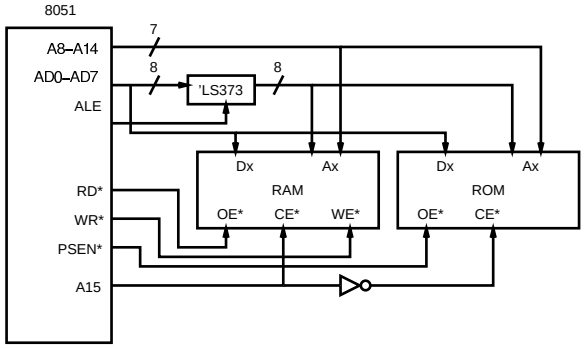
The design you are to analyze consists of: (1) an Intel 80C51BH microcontroller operating at 12 MHz with external memory, (2) an NEC μPD43256B-B15 150ns 32k $\times$ 8 RAM, and (3) a Texas Instruments TMS27C256-250 250ns 32k $\times$ 8 EPROM.

The data sheets for these devices are available in PDF format at the following URLs:

- `http://developer.intel.com/design/mcs51/datashts/27041907.pdf`
- `http://www.ic.nec.co.jp/english/pdf/M10770EJ9V0DS00.pdf`
- `http://www-s.ti.com/sc/psheets/smls256h/smls256h.pdf`

For this assignment you'll only need the introductory material and the timing specifications from each data sheet.

The circuit to be analyzed is:



The 8051 uses a Harvard architecture which means that the program and data memories have separate address spaces. The 8051's PSEN* line indicates whether the current access is to program or data memory.

When the 8051 is used with external memory "port 0" is used for both the LS 8 bits of the data and address busses and "port 2" is used for the MS 8 bits of the address.

Like some other processors, the 8051 multiplexes the least significant 8 bits of the address bus and the 8 bits of the data bus. The 8051's ALE output is used to control an external 8-bit latch (a 74LS373) which loads the LS 8 address bits from the multiplexed bus during the first part of a read or write cycle and then holds the LS 8 bits of the address value during the rest of the cycle while the same CPU pins are used to read or write data. Note that the latch is transparent when its control input is high and the data is latched when it goes low.

The remaining connections are straightforward: RD* drives the RAM's output enable (OE*) and WR* drives the RAM's write enable (WE*). PSEN* drives the EPROM's OE*. Chip selects are driven by the A15 address line and it's complement.

Verify whether this design will meet the timing requirements of the 8051 and the RAM for both read and write cycles to the RAM and read cycle to the EPROM. First determine which of the chips' specifications are timing requirements. Then obtain an expression for each timing requirement as a function of the guaranteed responses and the clock periods and compute the margin available for each requirement. If any of the requirements are not met, find the maximum 8051 clock period and frequency for at which that requirement would be met. Note any requirements for which it is not possible to determine if they are met.

You can assume the following: the clock is running at exactly 12 MHz, the clock has a 50% duty cycle, the 74LS373 latch timing requirements will be met, and that both the latch and the inverter have a negligible propagation delay.