Assignment 5

Due February 23, 1998

This assignment asks you to design two memory systems including address decoding.

Question 1

Draw the schematic of a 32 kByte RAM memory system for an 8-bit CPU using 16k by 4 devices. Assume the CPU has a 24-bit address bus (A0 to A23), an 8-bit data bus (D0 to D7), and RD* and WR* read/write signals. Each memory chip has four bi-directional data pins (Q0 through Q3), address inputs (A0, A1, ...), an active-high chip-select signal (CS) and an active-low write strobe (W*). The RAM's CS inputs should be driven by an address decoding circuit and W* should be driven from the CPU's WR* signal. Show all connections between the CPU, the address decoder and the memory chips. The internal details of the address decoder need not be shown.

You may use the bus notation X[n:m] to indicate a subset of the signals of X consisting of bits n through m. For example, the following diagram shows that D2 connects to Q6 and D3 connects to Q7:

To avoid ambiguity, place pin (signal) labels inside the rectangles representing the chips and the corresponding bus labels outside.

Question 2

Write VHDL descriptions of an address decoder for the memory systems above so that the 32k RAM bank appears at addresses from FF8000H to FFFFFFH and also from 008000H to 00FFFFH, but in no other places in memory. The entity statement for your decoder should be as follows:

```
entity decoder is
   port (
   a : in std_logic_vector (X to Y) ;
   e : out std_logic_vector (A to B) ) ;
end decoder ;
```

where a is the address input and e are the enables for the different memory banks. A, B, X, and Y should be the appropriate values from question 1. Synthesize your design and hand in a listing and a schematic of the resulting circuit. You need not simulate your design.

Question 3

Draw the schematic of a memory system using RAM and EPROM for a 16-bit CPU using four 32k by 8 SRAMs and eight 16k by 4 EPROMs. Assume the CPU always accesses memory 16 bits at a time and has a 20-bit address bus (of which only A1 to A19 are visible outside the CPU), a 16-bit data bus (D0 to D15) and RD* and WR* read/write signals. The CPU uses conventional byte addressing (each byte is addressable). Each memory chip has bi-directional data in/out pins (Q0 to Q7 or Q0 to Q3), address inputs (A0, A1, ...) and an active-low chip-select signal (CS*). The RAMs also have active-low write strobes (W*). The CS* pins should be driven from an address decoding circuit and W* should be driven from the CPU's WR* signal. You may assume all memory chips' outputs are tri-stated when the CS* is not asserted. Show all connections between the CPU and the memory chip pins. You may use the bus notation described above. The details of the address decoder need not be shown.

Question 4

Design two address decoders for the circuit described above. The first design should use two 3 to 8 decoders (as described in the data sheet from assignment 1) and inverters. The second should be a synthesizable circuit description in VHDL.

The decoders should place the RAM starting at memory location 0 and the EPROM at memory lo-

cation F0000H. Both decoders should fully decode CPU addresses.

For the design that uses a 3 to 8 decoder draw a schematic showing how the inputs and outputs are connected to the address bus and to the memory chip's `CS*` inputs. Note that the 3-to-8 decoder has three enable inputs which must be asserted for any of the outputs to be asserted.

For the VHDL-based designs write an entity and an architecture. Use `std_logic_vector`-type input signal named `A` with an appropriate `downto` range and as many active-low `std_logic`-type outputs signals named `ROMCSi_N` and `RAMCSi_N` (i=0,1,...) as are required by your design. Synthesize your design and hand in a listing and a schematic of the resulting circuit. You need not simulate your design.