ELEC 379 : MICROCOMPUTER SYSTEM DESIGN
1997/98 WINTER SESSION TERM 2

Assignment 2 - VHDL Synthesis

due February 4, 1998

Question 1

In this assignment you will design, simulate and synthesize an 8-bit bidirectional shift register. This particular device allows parallel read/write access to the shift register over a tri-state bus.

Start by retrieving the data sheet for the Motorola MC74AC323 from `http://motserv.indirect.com/logic/dl138.html` and printing pages 1 and 3. Read the description of the device. Make sure you understand *all* aspects of the operation of the device.

Use the following entity declaration for your design:

```
entity MC74AC323 is
   port (
   io : inout std_logic_vector (0 to 7) ;
   s0, s1, oe1, oe2, ds0, ds7, cp, sr : in std_logic ;
   q0, q7 : out std_logic ) ;
end  MC74AC323 ;
```

Write a synthesizeable architecture that duplicates the behaviour of the MC74AC323.

Note the following:

- the `io` port is bidirectional and tri-stateable
- the `io` array indices are in ascending order
- you'll need to use `std_logic_1164` package
- assume positive-true logic (0 = L, 1 = H)
- the output enables and the synchronous reset are active-low

Include comments in your code as described the previous assignment.

Read the instructions on the course web page describing how to simulate a VHDL description using the Synopsys VSS simulator. Use the test bench in the file `~elec379/asg2tb.vhd` to test your design.

When your design simulates without errors, synthesize your design using Synopsys Design Compiler and plot a schematic of the result.

Hand in the following:

- your VHDL code
- the log of your simulation
- the schematic of your synthesized circuit