Assignment 1 - VHDL Synthesis

due January 26, 1997

Question 1

In this assignment you'll write a VHDL circuit description and synthesize it into a schematic.

Point your favourite Web browser at:

`http://www.national.com/pf/MM/MM74HCA138.html`

and retrieve the 6-page data sheet for the MM74HCA138 3-to-8 decoder in PDF format. The first page contains the device's truth table. Print this page.

Write a VHDL entity statement for this device. Use the same signal names (e.g. `a`, `g2a`, `y`, etc) as used in the data sheet. Use the `bit` type for the six inputs and the `bit_vector` type with indices `(7 downto 0)` for the `y` output. Ignore power (Vcc) and ground. Use your initials plus the digits 138 as the entity name (e.g. if your name is Doug Mah, your entity statement would begin "`entity DM138 is` ...").

Write an architecture that models the behaviour of the device. Assume positive true logic (0 = L, 1 = H). Note that the outputs are active-low, the inputs are active-high and the `a` input is the "least-significant" input. Don't worry if your description ends up looking rather long-winded.

Include comments giving at least the purpose of the circuit ("3 to 8 decoder"), your name and student number, the course and the date.

Look up the instructions on using Design Compiler available on the course Web page. Synthesize your design using Synopsys Design Compiler and plot a schematic of the result. Since this is a combinational circuit your design should not have any flip-flops (if it does, check the paragraph you highlighted in lecture 2).

Hand in a listing of your VHDL code and the resulting schematic.