THE UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
EECE 379 : Microcomputer System Design
1999/2000 Winter Session Term 2

MID-TERM EXAMINATION
8:30 – 9:20 AM
February 25 2000

This exam has two (2) questions. The marks for each question are as indicated. There are a total of 22 marks. Answer all questions. Write your answers in the exam book provided. Show your work. You may answer the questions in any order. Books, notes and calculators are allowed. You may keep this exam paper.

Question 1 (11 marks)

This question asks you to design the digital electronics for a device that measures the depth of the water under a ship.

The device transmits a signal from the bottom of the ship. Some time later it receives the echo from the sea floor. By measuring the delay between transmitting the pulse and receiving the echo, your device can determine the depth.

Your device has the following inputs and outputs:

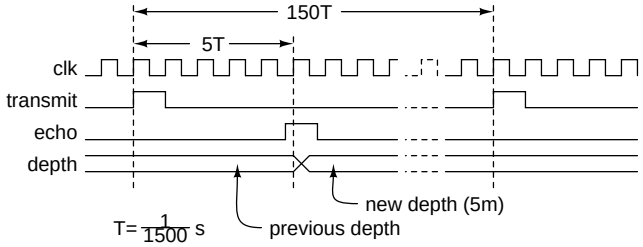
- a 1500 Hz clock input, `clk`
- and active-high input, `echo`, that indicates an echo is being received
- an active-high output, `transmit`, that turns on the transmitter
- an 8-bit output, `depth`, that indicates the depth in metres

Your device should transmit one pulse every 100 milliseconds (ten times per second). Each pulse should have a duration of $\frac{1}{1500}$ seconds. When the echo is received your device should output the newly-measured depth and hold it until the next depth measurement is available.

The speed of sound in water is approximately 1500 m/s. Since the clock rate is 1500 Hz, the number of clock cycles elapsed since the start of the transmitted pulse indicates the depth in metres.

You can assume that there will always be an echo and that it will last for exactly one clock period.

The following diagram shows an example of the input and output waveforms:



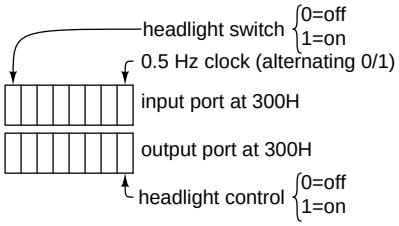
Write a VHDL entity and architecture for a circuit that is synthesizeable by MaxPlus+II and meets these specifications. You may use `std_logic`, `std_logic_vector` or `unsigned` types. Apply type conversion functions as necessary. Any `process` in your VHDL code must contain exactly one `if` statement controlling one or more simple signal assignment statements. You need not include comments. Include any `library` and `use` statements required. You need not synchronize inputs or register outputs (for glitch removal).

Hint: You will need at least two registers, one to hold the output and one to implement a counter.

Question 2 (11 marks)

This question asks you to write an 80x86 assembly-language program that implements a car headlight controller. This controller implements a delay feature so that the headlights stay on for 30 seconds after the driver turns the headlight switch off.

The interface between your program and the hardware is through two 8-bit ports (one input port and one output port). Both ports are at i/o (not memory) address 300H. The LS bit of the input port is a signal that alternates between 0 and 1 every second (i.e. the frequency of the signal is 0.5 Hz). The MS bit of the input port indicates the headlight switch position: 1 for "on" and 0 for "off". The LS bit of the output port actually controls the headlights: 1 turns them on and 0 turns them off:



Your program should run continuously. It should turn the headlights on when the driver turns the switch on. After the driver turns the switch off, there should be a delay of between 30 and 31 seconds and then the headlights should be turned off. The driver should be able to turn the headlights back on during this delay time. The headlights should come on within a very short time ($\ll 1$ s) of the switch being turned on.

You must declare storage for any temporary variables you use, but you need not include comments or assembler directives such as `segment`, `assume` or `org`.

Hints: Write a pseudo-code, flowchart, or other high-level solution before you start coding! Use functions.