Solution to Assignment 5
Timing Analysis

Question 1

(a)

To implement a 16-bit data bus using 8-bit wide RAMs requires 16/8=2 chips per bank. Each bank supplies 64k x 2 = 128k Bytes. This memory system requires 384k/128k=3 banks.

The schematic is given in figure 1.

(b)

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-- ELEC 379 Assignment 5 Solutions
-- Ed Casas, April 6, 2000
-- Memory Decoder for 386SX Example

library ieee ;
use ieee.std_logic_1164.all ;

entity sol5 is
   port (
   -- address
   a : in std_logic_vector (23 downto 17) ;
   -- r/w*, BHE*, BLE*
   rw, bhe, ble : in std_logic ;
   -- RD*, WR*, active-low chip selects
   rd, wr, cs2h, cs2l, cs1h, cs1l,
      cs0h, cs0l : out std_logic ) ;
end sol5 ;

architecture rtl of sol5 is
   signal aok, cs2, cs1, cs0 : std_logic ;
begin
   -- memory system addressed
   aok <= '1' when a(23 downto 19) = "00000" else '0' ;

   -- bank selects
   cs2 <= '1' when aok = '1' and a(18 downto 17) = "10"
      else '0' ;
   cs1 <= '1' when aok = '1' and a(18 downto 17) = "01"
      else '0' ;
   cs0 <= '1' when aok = '1' and a(18 downto 17) = "00"
      else '0' ;

   -- chip selects
   cs2h <= '0' when cs2 = '1' and bhe = '0' else '1' ;
   cs2l <= '0' when cs2 = '1' and ble = '0' else '1' ;
   cs1h <= '0' when cs1 = '1' and bhe = '0' else '1' ;
   cs1l <= '0' when cs1 = '1' and ble = '0' else '1' ;
   cs0h <= '0' when cs0 = '1' and bhe = '0' else '1' ;
   cs0l <= '0' when cs0 = '1' and ble = '0' else '1' ;

   -- decoded read and write strobes
   rd <= '0' when rw = '1' else '1' ;
   wr <= '0' when rw = '0' else '1' ;

end rtl ;
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Question 2

For each device we need to consider both reads and writes from/to all possible devices. For each combination we check the all timing requirements.

All times in nanoseconds. Note that if the margin is zero the specification is met.

CPU Requirements

The ACK signal is ignored in this design. Therefore ACK is not an input. Since timing requirements are timing specifications that end on an input signal, the specifications related to the ACK are not requirements. This leaves four requirements: t_{DAD}, t_{DRLD}, t_{HDA} and t_{HDRH}.

As specified in the question, the timing analysis assumes DT=W=HI=0.

Note that in this circuit there are two separate timing requirements implied by t_{DAD}. One is the access time (delay from address to data valid), the second is the chip enable delay (from MSx* to data valid).

Read (Flash)

The timing analysis is given in Table 1.

Read (RAM)

The timing analysis is given in Table 2.

Write (Both)

During a write cycle none of the CPU signals is an input (ACK is not an input for the reasons explained above) and therefore there are no timing requirements.

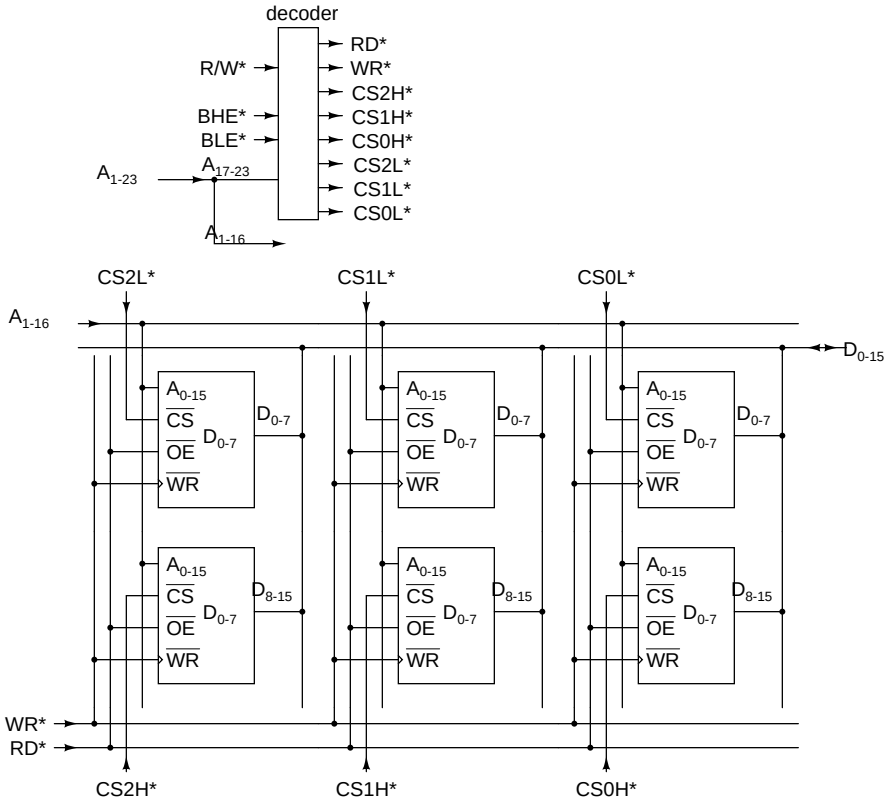

Figure 1: Memory system schematic.

requirement			guaranteed		
name	symbol	value	expression	value	margin
Data Delay from RD*	t_{DRLD}	< 24	t_{OE}	< 40	-16
Data Delay from Address	t_{DAD}	< 28	t_{ACC}	< 70	-42
			t_{CE}	< 70	-42
Data Hold from Address	t_{HDA}	> 0	t_{OH}	> 0	0
			t_{DF}	> 0	0
Data Hold from RD*	t_{HDRH}	> 0	t_{DF}	> 0	0

Table 1: CPU Requirements, Flash Read.

RAM Requirements

Read

The only requirement is the read cycle time. This is not given directly on the data sheets but is likely to be the same as the duration of a bus cycle. It can also be calculated as the sum of several minimums as shown below (although a note in the data sheet discourages us from doing this sort of analysis).

The timing analysis is given in Table 3.

Write

In this design the data bus output is controlled by OE* (the CPU's RD* signal) so the first timing diagram applies ("Write Cycle 1"). The second timing diagram applies to systems where OE* is left asserted and the output is controlled by CS*.

As above, the minimum write cycle time should be computed directly, if possible, rather than by adding up minimums as is shown below.

The RAM write cycle ends when either CS* or

requirement			guaranteed		
name	symbol	value	expression	value	margin
Data Delay from RD*	t_{DRLD}	< 24	t_{OE}	< 12	12
Data Delay from Address	t_{DAD}	< 28	t_{AA}	< 25	3
			t_{ACS}	< 25	3
Data Hold from Address	t_{HDA}	> 0	t_{OH}	> 3	3
			t_{CHZ}	> 0	0
Data Hold from RD*	t_{HDRH}	> 0	t_{OHZ}	> 0	0

Table 2: CPU Requirements, RAM Read.

requirement			guaranteed		
name	symbol	value	expression	value	margin
Read Cycle	t_{RC}	> 25	$t_{DARL}+t_{RW}+t_{DRHA}$	$> 3+25-1$ $= 27$	2

Table 3: RAM Requirements, CPU Read.

requirement			guaranteed		
name	symbol	value	expression	value	margin
Write Cycle	t_{WC}	> 25	$t_{DAWH}+t_{DWHA}$	$> 29+0$ $= 29$	4
Address Width	t_{AW}	> 15	$t_{DAWH}+t_{DWHA}$	> 29	14
Select Width	t_{CW}	> 15	$t_{DAWH}+t_{DWHA}$	> 29	14
Address Setup	t_{AS}	> 0	t_{DAWL}	> 3.5	3.5
Write Width	t_{WP}	> 15	t_{WW}	> 24.5	9.5
Address Hold	t_{WR}	> 0	t_{DWHA}	> 0	0
Data Setup	t_{DW}	> 10	t_{DDWH}	> 15.5	5.5
Data Hold	t_{DH}	> 0	t_{DATRWH}	> 1	1

Table 4: RAM Requirements, CPU Write.

WE* goes inactive.

The timing analysis is given in Table 4.

Flash Requirements

The flash has no read-cycle timing requirements.