Assignment 5
Memory Design and Timing Analysis

due Wednesday, March 29 2000

There was no assignment titled "Assignment 4." Instead the second part of Assignment 3 will be counted as Assignment 4.

Question 1

Design a RAM memory system for a 386SX CPU (16-bit data bus, 24-bit address bus) using 64kx8 SRAMs. The total memory size should be 384 kBytes. Each RAM chip has address (A_i), CS* (chip select), OE* (output enable), and WE* (write strobe) inputs and a bidirectional data bus (D_{7-0}).

(a) Compute the number of RAM chips required and draw a schematic showing unambiguously how the address, OE*, WE*, CS* and data bus signals would be connected. You can assume the presence of the circuit described in (b).

(b) Write a VHDL entity and architecture that describe a logic circuit that generates CS*, OE* and WE* signals. The inputs will be the CPU address bus, W/R*, BHE* and BLE*.

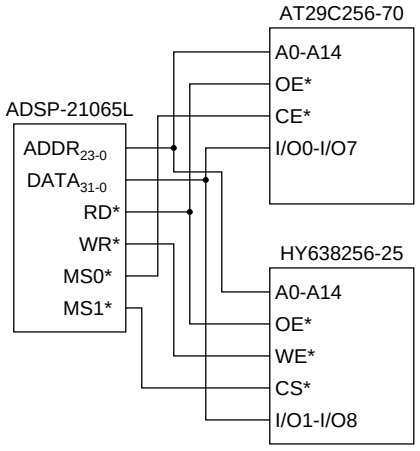
You need not worry about signal timing for this question.

Question 2

This question asks you to analyze the timing requirements for the CPU and memory devices in a small microcomputer system. The design consists of:

1. an Analog Devices ADSP-21065L "SHARC" microprocessor operating at 30 MHz,
2. a Hyundai Hy638256-25 32k $\times$ 8 SRAM, and
3. two Atmel AT29C256-70 32k $\times$ 8 'flash' EEPROMs

connected as shown below:



The full manufacturer's data sheets for these devices can be retrieved from:

1. `http://www.analog.com/pdf/ADSP-21065L_a.pdf`
2. `http://kcs.hei.co.kr/models/sram/sramcomp/38256.PDF`
3. `http://www.atmel.com/atmel/acrobat/doc0046.pdf`

although you'll only need to print out the signal definitions, timing specifications and timing diagrams. These pages are available on the course Web page.

The CPU clock frequency is 30 MHz (t_{CK}=33.3ns) and you may assume that it has been configured for no wait states, address hold or bus idle cycles (W=DT=HI=0). The ACK CPU input signal is not used.

In this design the flash is read-only. The SRAM is enabled (CS*) by the MS1* and the flash is enabled (CE*) by MS0* "memory strobe" signals from the CPU. The SRAM write enable (WE*) is controlled by the CPU's R/W* signal. The SRAM and flash tri-state outputs (OE*) are enabled by RD*. Since the CPU has a 32-bit data bus there are actually four devices in each bank but this does not affect the timing analysis.

Prepare a table of timing requirements for each IC for each type of cycle (read or write). Include in your table only the timing requirements, not the guaranteed responses. You might find the following steps helpful in identifying all the timing requirements:

1. identify the input signals in each timing diagram
2. on each of these signals, mark the timing specifications that *end* on an input signal edge

Create a table, as shown in the course notes, showing the timing analysis for each timing requirement. For each cycle, obtain an *equation* for each timing requirement as a function of the guaranteed responses and then compute the margin available for each requirement (negative if the requirement is not met).

Identify any requirements where it is not possible to determine if the requirements are met.

Some timing requirements actually represent two (or more) different requirements with the same values. Use two lines in the table for these cases.

There appears to be a typo in the RAM data sheet – assume t_{WR} for the -25 part is 0 ns.

A more detailed timing analysis would also consider consecutive read and write cycles to ensure that bus conflicts did not occur. You need not do this for this assignment.

Your answer should include tables for each combination of device and bus cycle that has timing requirements.