

MOS INTEGRATED CIRCUIT μ PD43257B

256K-BIT CMOS STATIC RAM 32K-WORD BY 8-BIT

Description

The μ PD43257B is a high speed, low power, and 262,144 bits (32,768 words by 8 bits) CMOS static RAM. Battery backup is available (L, LL versions). And this product has two chip enable pins ($\overline{\text{CE1}}$, CE2) to extend the capacity.

The μ PD43257B is packed in 28-pin plastic DIP and 28-pin plastic SOP.

Features

• 32,768 words by 8 bits organization

• Fast access time: 70, 85 ns (MAX.)

• 2 V (MIN.) data retention

• Two chip enable inputs: CE1, CE2

| Part number | Access time ns (MAX.) | Operating supply voltage | Operating temperature °C | Standby supply current µA (MAX.) | Data retention supply current μA (MAX.) |
|--------------|--------------------------|--------------------------|--------------------------------|-------------------------------------|---|
| μPD43257B-L | 70, 85 | 4.5 to 5.5 | 0 to 70 | 50 | 3 |
| μPD43257B-LL | | | | 15 | 2 |

Note TA ≤ 40 °C, Vcc = 3 V

★ Version X

This Data sheet can be applied to the version X. This version is identified with its lot number. Letter X in the fifth character position in a lot number signifies version X.



The information in this document is subject to change without notice.



Ordering Information

| Part number | Package | Access time | Supply curre | nt μA (MAX.) | Remark |
|------------------|---------------------------------|-------------|--------------|------------------------|------------|
| T dit Hambol | rackage | ns (MAX.) | At standby | At data retention Note | Roman |
| μPD43257BCZ-70L | 28-pin plastic | 70 | 50 | 3 | L Version |
| μPD43257BCZ-85L | DIP (600 mil) | 85 | | | |
| μPD43257BCZ-70LL | | 70 | 15 | 2 | LL Version |
| μPD43257BCZ-85LL | | 85 | | | |
| μPD43257BGU-70L | 28-pin plastic SOP (450 mil) | 70 | 50 | 50 3 | |
| μPD43257BGU-85L | 30F (450 IIII) | 85 | | | |
| μPD43257BGU-70LL | | 70 | 15 | 2 | LL Version |
| μPD43257BGU-85LL | | 85 | | | |

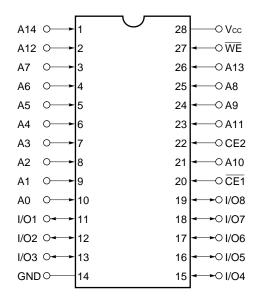
Note TA \leq 40 °C, Vcc = 3 V



Pin Configuration (Marking Side)

28-pin plastic DIP (600 mil) $[\mu PD43257BCZ]$

28-pin plastic SOP (450 mil) [μ PD43257BGU]



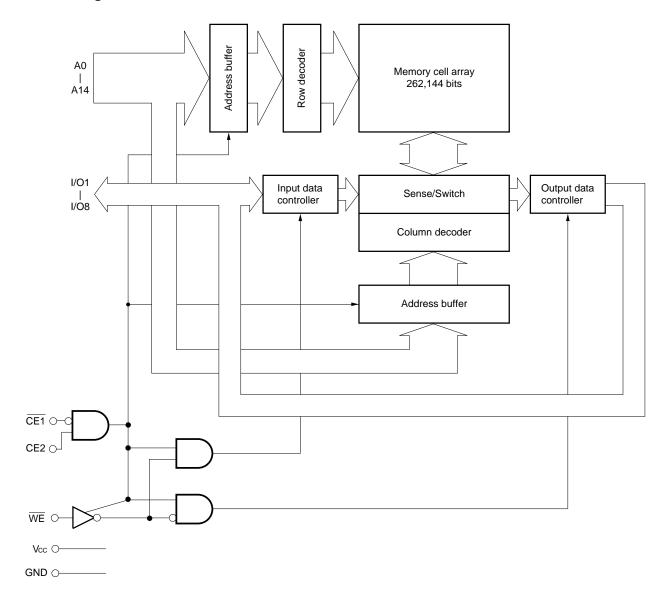
A0 - A14 : Address inputs I/O1 - I/O8 : Data inputs/outputs

CE1 : Chip Enable1
CE2 : Chip Enable2
WE : Write Enable
Vcc : Power supply

GND : Ground



Block Diagram



Truth Table

| CE1 | CE2 | WE | Mode | I/O | Supply current |
|-----|-----|----|--------------|----------------|----------------|
| Н | × | × | Not selected | High impedance | Isв |
| × | L | × | | | |
| L | Н | Н | Read | Dout | ICCA |
| L | Н | L | Write | Din | |

Remark ×: Don't care



Electrical Characteristics

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|--|--------|-----------------------------------|------|
| Supply voltage | Vcc | -0.5 ^{Note} to +7.0 | V |
| Input/Output voltage | VT | -0.5 ^{Note} to Vcc + 0.5 | V |
| Operating ambient temperature T _A | | 0 to 70 | °C |
| Storage temperature | Tstg | −55 to +125 | °C |

Note -3.0 V (MIN.) (Pulse width 50 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|-------------------------------|--------|----------------------|------|-----------|------|
| Supply voltage | Vcc | 4.5 | 5.0 | 5.5 | V |
| High level input voltage | VIH | 2.2 | | Vcc + 0.5 | V |
| Low level input voltage | VIL | -0.3 ^{Note} | | +0.8 | V |
| Operating ambient temperature | ТА | 0 | | 70 | °C |

Note −3.0 V (MIN.) (Pulse width 50 ns)



DC Characteristics (Recommended operating conditions unless otherwise noted)

| | Davamatas | Caab al | Took Com | . diki a a a | μΡΕ |)43257 | 'B-L μPD4325 | | 43257 | B-LL | l lait |
|---|---------------------------|------------------|---|--|---------|--------|--------------|---------|-------|------|--------|
| | Parameter | Symbol | Test Cor | rest definitions | | TYP. | MAX. | MIN. | TYP. | MAX. | Unit |
| | Input leakage current | lu | V _{IN} = 0 V to V _{CC} | | -1.0 | | +1.0 | -1.0 | | +1.0 | μΑ |
| | I/O leakage current | ILO | $\frac{V_{I/O}}{CE1} = 0 \text{ V to Vcc},$ $\frac{V_{I/O}}{CE2} = V_{IH} \text{ or CE2} = V_{II}$ | $\frac{V_{VO}}{CE1} = 0 \text{ V to Vcc},$ $\frac{V_{IVO}}{CE1} = V_{IH} \text{ or } CE2 = V_{IL} \text{ or } \overline{WE} = V_{IL}$ | | | +1.0 | -1.0 | | +1.0 | μΑ |
| | Operating supply current | ICCA1 | CE1 = VIL, CE2 = VIH, Minimum cycle time, | μPD43257B-70 | | | 45 | | | 45 | mA |
| | current | | I _{1/0} = 0 mA | μPD43257B-85 | | | 45 | | | 45 | |
| | | Icca2 | $\overline{\text{CE1}} = \text{V}_{\text{IL}}, \text{CE2} = \text{V}_{\text{IH}}, \\ I_{\text{I/O}} = 0 \text{ mA}$ | | | | 10 | | | 10 | |
| | | Іссаз | $\overline{\text{CE1}} \leq 0.2 \text{V}$, $\text{CE2} \geq \text{Vcc} - 0.2 \text{V}$, $\text{Cycle} = 1 \text{ MHz}$, $\text{V}_{\text{IL}} \leq 0.2 \text{ V}$, $\text{V}_{\text{IH}} \geq \text{Vcc} - 0.2 \text{ V}$, $\text{I}_{\text{I/O}} = 0 \text{mA}$ | | | | 10 | | | 10 | |
| | Standby supply current | lsв | CE1 = VIH, CE2 = VIL | | | | 3 | | | 3 | mA |
| * | current | I _{SB1} | $\overline{\text{CE1}} \ge \text{Vcc} - 0.2 \text{ V},$ $\text{CE2} \ge \text{Vcc} - 0.2 \text{ V}$ | | | 1.0 | 50 | | 0.5 | 15 | μΑ |
| * | | I _{SB2} | CE2 ≦ 0.2 V | | | 1.0 | 50 | | 0.5 | 15 | |
| | High level output voltage | V _{OH1} | Iон = -1.0 mA | | 2.4 | | | 2.4 | | | ٧ |
| | | V _{OH2} | Iон = -0.1 mA | | Vcc-0.5 | | | Vcc-0.5 | | | |
| | Low level output voltage | Vol | IoL = 2.1 mA | | | | 0.4 | | | 0.4 | > |

Remarks 1. VIN: Input voltage

2. These DC Characteristics are in common regardless of package types.

Capacitance (T_A = 25 $^{\circ}$ C, f = 1 MHz)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|--------|------------------------|------|------|------|------|
| Input capacitance | Cin | $V_{IN} = 0 V$ | | | 5 | pF |
| Input/Output capacitance | C1/0 | V _{1/O} = 0 V | | | 8 | pF |

Remarks 1. Vin: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

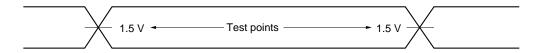


AC Characteristics (Recommended operating conditions unless otherwise noted)

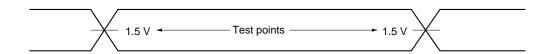
AC Test Conditions

Input waveform (Rise/fall time ≤ 5 ns)

Input pulse levels: 0.8 V to 2.2 V

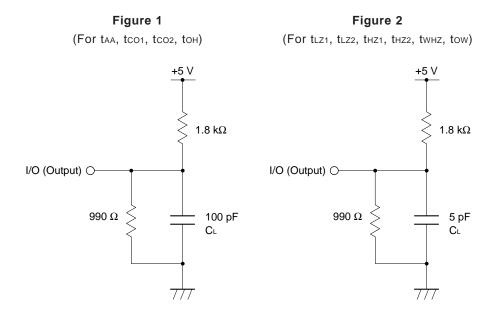


Output waveform



Output load

AC characteristics with notes should be measured with the output load shown in Figure 1 and Figure 2.



Remark C_L includes capacitances of the probe and jig, and stray capacitances.



Read Cycle

| Parameter | Cymhol | μPD432 | 257B-70 | μPD432 | 257B-85 | Unit | Condition | |
|---------------------------------|--------|--------|---------|--------|---------|-------|-----------|--|
| Farameter | Symbol | MIN. | | MIN. | MAX. | Offic | Condition | |
| Read cycle time | trc | 70 | | 85 | | ns | | |
| Address access time | tAA | | 70 | | 85 | ns | | |
| CE1 access time | tco1 | | 70 | | 85 | ns | Note 1 | |
| CE2 access time | tCO2 | | 70 | | 85 | ns | Note 1 | |
| Output hold from address change | tон | 10 | | 10 | | ns | | |
| CE1 to output in low impedance | tLZ1 | 10 | | 10 | | ns | | |
| CE2 to output in low impedance | tLZ2 | 10 | | 10 | | ns | | |
| CE1 to output in high impedance | tHZ1 | | 30 | | 30 | ns | Note 2 | |
| CE2 to output in high impedance | tHZ2 | | 30 | | 30 | ns | | |

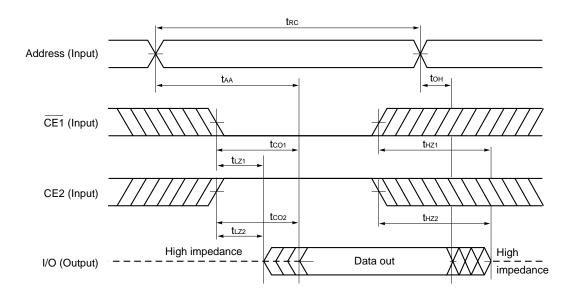
See the output load shown in Figure 1.

2. See the output load shown in Figure 2.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Read Cycle Timing Chart

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Remark In read cycle, $\overline{\text{WE}}$ should be fixed to high level.

NEC



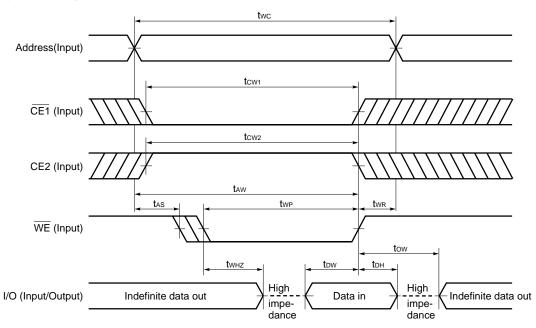
Write Cycle

| Doromotor | Cymbal | μPD432 | :57B-70 | μPD432 | 257B-85 | Unit | Condition |
|---------------------------------|--------|--------|---------|--------|---------|------|-----------|
| Parameter | Symbol | MIN. | MAX. | MIN. | MAX. | Unit | |
| Write cycle time | twc | 70 | | 85 | | ns | |
| CE1 to end of write | tcw1 | 50 | | 70 | | ns | |
| CE2 to end of write | tcw2 | 50 | | 70 | | ns | |
| Address valid to end of write | taw | 50 | | 70 | | ns | |
| Write pulse width | twp | 55 | | 65 | | ns | |
| Data valid to end of write | tow | 30 | | 35 | | ns | |
| Data hold time | tDH | 0 | | 0 | | ns | |
| Address setup time | tas | 0 | | 0 | | ns | |
| Write recovery time | twr | 0 | | 0 | | ns | |
| WE to output in high impedance | twHZ | | 30 | | 30 | ns | Nete |
| Output active from end of write | tow | 10 | | 10 | | ns | Note |

Note See the output load shown in Figure 2.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Write Cycle Timing Chart 1 (WE Controlled)

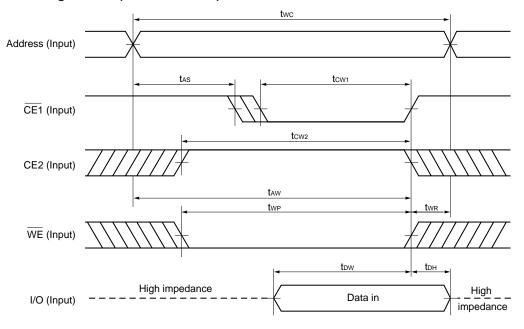


- Cautions 1. During address transition, at least one of pins $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, $\overline{\text{WE}}$ should be inactivated.
 - 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.
- **Remarks 1.** Write operation is done during the overlap time of a low level $\overline{CE1}$, \overline{WE} , and a high level CE2.
 - 2. If CE1 changes to low level at the same time or after the change of WE to low level, or if CE2 changes to high level at the same time or after the change of WE to low level, the I/O pins will remain high impedance state.
 - 3. When WE is at low level, the I/O pins are always high impedance. When WE is at high level, read operation is executed. Therefore OE should be at high level to make the I/O pins high impedance.

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Write Cycle Timing Chart 2 (CE1 Controlled)

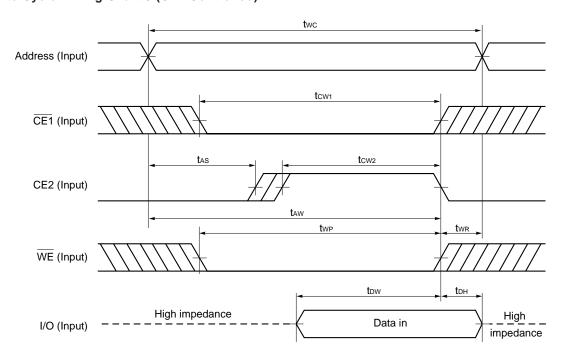


Cautions 1. During address transition, at least one of pins CE1, CE2, WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level $\overline{CE1}$, \overline{WE} , and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins CE1, CE2, WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level $\overline{CE1}$, \overline{WE} , and a high level CE2.



Low Vcc Data Retention Characteristics

L Version (μ PD43257B-L: T_A = 0 to 70 °C)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|---|------|------|---------|------|
| Data retention supply voltage | Vccdr1 | <u>CE1</u> ≧ Vcc – 0.2 V, CE2 ≧ Vcc – 0.2 V | 2.0 | | 5.5 | V |
| | Vccdr2 | CE2 ≦ 0.2 V | 2.0 | | 5.5 | |
| Data retention supply current | ICCDR1 | Vcc = 3.0 V, CE1 ≧ Vcc - 0.2 V, | | 0.5 | 20 Note | μΑ |
| | | CE2 ≧ Vcc - 0.2 V | | | | |
| | Iccdr2 | Vcc = 3.0 V, CE2 ≦ 0.2 V | | 0.5 | 20 Note | |
| Chip deselection to data retention mode | tcdr | | 0 | | | ns |
| Operation recovery time | tr | | 5 | | | ms |

Note 3 μ A (T_A \leq 40 °C)

LL Version (μ PD43257B-LL: T_A = 0 to 70 °C)

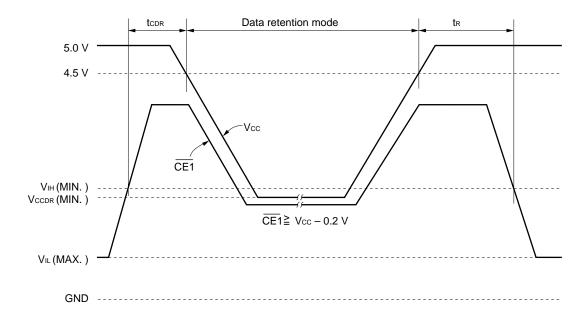
| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|--------|---|------|------|--------|------|
| Data retention supply voltage | Vccdr1 | <u>CE1</u> ≧ Vcc – 0.2 V, CE2 ≧ Vcc – 0.2 V | 2.0 | | 5.5 | V |
| | Vccdr2 | CE2 ≦0.2 V | 2.0 | | 5.5 | |
| Data retention supply current | ICCDR1 | Vcc = 3.0 V, CE1 ≧ Vcc - 0.2 V, | | 0.5 | 7 Note | μΑ |
| | | CE2 ≧ Vcc - 0.2 V | | | | |
| | ICCDR2 | Vcc = 3.0 V, CE2 ≦ 0.2 V | | 0.5 | 7 Note | |
| Chip deselection to data | tcdr | | 0 | | | ns |
| retention mode | | | | | | |
| Operation recovery time | tr | | 5 | | | ms |

Note 2 μ A (T_A \leq 40 °C), 1 μ A (T_A \leq 25 °C)



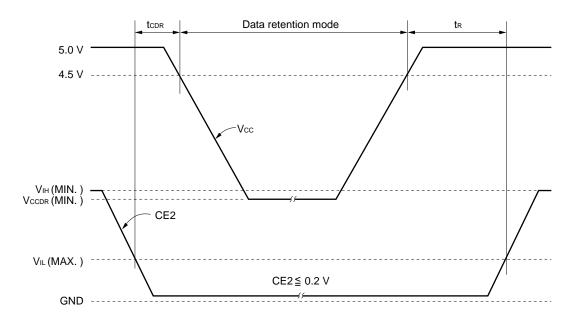
Data Retention Timing Chart

(1) CE1 Controlled



Remark On the data retention mode by controlling $\overline{CE1}$, the input level of CE2 must be CE2 \geq Vcc - 0.2 V or CE2 \leq 0.2 V. The other pins (Address, I/O, \overline{WE}) can be in high impedance state.

(2) CE2 Controlled

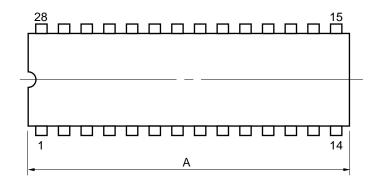


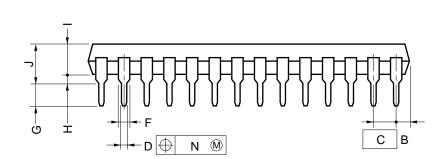
Remark The other pins $(\overline{CE1}, Address, I/O, \overline{WE})$ can be in high impedance state.

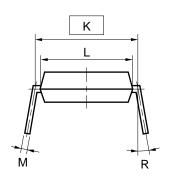


Package Drawings

28 PIN PLASTIC DIP (600 mil)







NOTES

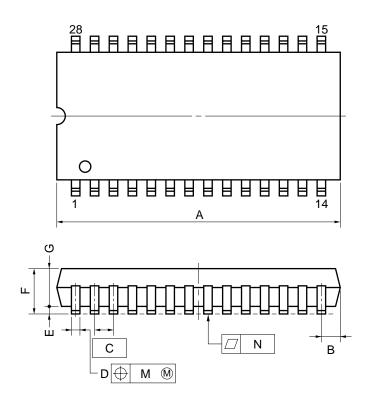
- Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|------|--|---------------------------|
| Α | 38.10 MAX. | 1.500 MAX. |
| В | 2.54 MAX. | 0.100 MAX. |
| С | 2.54 (T.P.) | 0.100 (T.P.) |
| D | 0.50±0.10 | 0.020+0.004 |
| F | 1.2 MIN. | 0.047 MIN. |
| G | 3.6±0.3 | 0.142±0.012 |
| Н | 0.51 MIN. | 0.020 MIN. |
| ı | 4.31 MAX. | 0.170 MAX. |
| J | 5.72 MAX. | 0.226 MAX. |
| K | 15.24 (T.P.) | 0.600 (T.P.) |
| L | 13.2 | 0.520 |
| М | 0.25 ^{+0.10} _{-0.05} | $0.010^{+0.004}_{-0.003}$ |
| N | 0.25 | 0.01 |
| R | 0 ~ 15° | 0 ~ 15° |
| | _ | |

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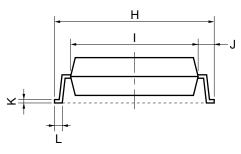


28 PIN PLASTIC SOP (450 mil)



detail of lead end





NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|------------------------|-----------------------------------|
| Α | 19.05 MAX. | 0.750 MAX. |
| В | 1.27 MAX. | 0.050 MAX. |
| С | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40±0.10 | $0.016^{+0.004}_{-0.005}$ |
| Е | 0.2±0.1 | 0.008±0.004 |
| F | 3.0 MAX. | 0.119 MAX. |
| G | 2.55±0.1 | $0.100^{+0.005}_{-0.004}$ |
| Н | 11.8±0.3 | 0.465 ^{+0.012} -0.013 |
| 1 | 8.4±0.1 | $0.331^{+0.004}_{-0.005}$ |
| J | 1.7±0.2 | 0.067±0.008 |
| K | $0.20^{+0.07}_{-0.03}$ | $0.008^{+0.003}_{-0.002}$ |
| L | 0.7±0.2 | $0.028^{+0.008}_{-0.009}$ |
| М | 0.12 | 0.005 |
| N | 0.10 | 0.004 |
| Р | 5°±5° | 5°±5° |

P28GU-50-450A-1



Recommended Soldering Conditions

The following conditions must be met when soldering μ PD43257B. For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C-10535E).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Type of Surface Mount Device

 μ PD43257BGU: 28-pin plastic SOP (450 mil)

Please consult with our sales offices.

Type of Through Hole Mount Device

 μ PD43257BCZ: 28-pin plastic DIP (600 mil)

| Soldering process | Soldering conditions |
|--------------------------------|--|
| Wave soldering (only to leads) | Solder temperature: 260 °C or below, Flow time: 10 seconds or below |
| Partial heating method | Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one lead) |

Caution Do not jet molten solder on the surface of package.

NEC μ PD43257B

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NEC μ PD43257B

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NOTES FOR CMOS DEVICES-

1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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