THE UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ELEC 379 : Microcomputer System Design
1998/99 Winter Session Term 1

MID-TERM EXAMINATION
12:30 pm – 1:20 pm
October 23, 1998

This exam has three (3) questions. The marks for each question are as indicated. There are a total of 30 marks. Answer all questions. Write your answers in the exam book provided. Show your work. You may answer the questions in any order. Books, notes and calculators are allowed. You may keep this exam paper.

Question 1 (10 marks)

Design a digital logic circuit to control the ignition system of a car engine. Your circuit has a clock input, `clk`, that receives one rising edge per degree of crankshaft rotation. Your circuit also has two one-bit inputs: the first, `tdc`, is asserted when the crankshaft angle is zero degrees and the second, `hispeed`, is asserted when the engine is operating at high speed. Your circuit has one output, `spark`, which turns on the spark plug when it is asserted. All inputs and outputs are active-high.

If the engine is operating at high speed, the `spark` output should be asserted when the crankshaft angle lies between 355 and 359 degrees. Otherwise the `spark` output should be asserted for crankshaft angles between 0 and 4 degrees.

Given the following VHDL entity declaration:

```
entity ignition is
begin
        port (
                clk : in std_logic ;
                tdc, hispeed : in std_logic ;
                spark : out std_logic ) ;
end ignition ;
```

write an architecture that implements this design that is synthesizeable by MaxPlus+II. Use type conversion functions as necessary. Any `process` in your VHDL code must contain exactly one `if` statement and one signal assignment statement. Do not repeat the entity declaration, do not include comments and do not worry about behaviour during the initial crankshaft revolution. Include any `library` and `use` statements required.

Hints: use a 9-bit register of type unsigned to represent the crankshaft angle. Note that the `std_logic_arith` package includes comparison operators for `unsigned` values.

Question 2 (10 marks)

Write a subroutine, `copyout:`, in 8086 assembly language that copies 64 bytes from memory to an output port at I/O port 220H. The 64 bytes are stored in a buffer starting at physical memory location 0C4000H. Your function must save and restore any registers it modifies before returning control to the calling function with a `RET` instruction. You must declare storage for any temporary variables you use, but you need not include comments or assembler directives such as `segment`, `assume` or `org`.

Question 3 (5 marks)

(a) Assume an address bus input signal has been declared as `a : std_logic_vector(15 downto 0)`. Write a VHDL expression (one statement) for an active-low bank-enable signal, `en`, that enables a 4 kB memory bank starting at address 4000H.

(b) An 80386SX CPU (16-bit data bus) executes the following operations:

```
mov     ax,1234
mov     [45],ax
mov     al,[46]
```

What memory location(s) will be altered by these instructions? How many write cycles will the CPU perform to complete these instructions? What will each location be set to? What is the final value of AX (in hex)?

(c) You are designing the memory system for a DSP microprocessor that requires 4 kB of external memory with a 20 ns access time (that's relatively fast). What type of RAM would you use? *Briefly* justify your choice.