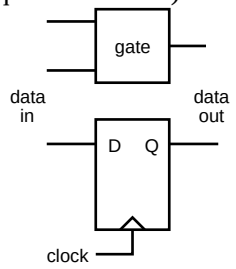
Timing Analysis

Timing analysis is the process of verifying that the timing requirements of each chip in a circuit are met. If this is not the case the circuit may operate erratically or not at all.
After this lecture you should be able to draw a timing diagram for a simple circuit, derive the expressions for a chip's timing requirements from the timing diagram and compute the margin for each requirement based on clock periods and the guaranteed responses of the other components.

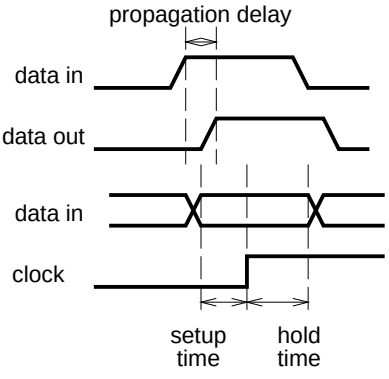
Timing Specifications

A chip's timing specifications are of two types: (1) timing requirements and (2) guaranteed responses. Guaranteed *responses*, such as propagation delays, are timing relationships between the chip's inputs and outputs (or possibly between two outputs) that the manufacturer guarantees will always be the case (assuming the chip is operated within it's recommended limits). Timing *requirements* are the time relationships between a chip's inputs that the chip's manufacturer states are required for the chip to operate properly.

The diagram below shows the simplest examples of the two types of circuits: a logic gate (an example of a combinational circuit) and a D flip-flop (an example of a sequential circuit):



and the diagram below shows the three most common timing specifications:



The most common guaranteed response is the *propagation delay* which is the maximum delay between a change in the input and the correct value appearing at the output.

The most common timing requirements are the *setup time* and *hold time* which are the minimum durations that the data input to a flip-flop has to be at the desired value before and after the relevant clock edge.

In addition to these 3 basic specifications many chips either require or guarantee a minimum or maximum *pulse width* or a minimum or maximum *cycle time* (waveform period).

Exercise: Which of these basic specifications would apply to a multiplexer? To a RAM chip? To a ROM?

Timing Analysis

Timing analysis will be part of every digital system design. After a preliminary circuit design the designer should verify that all of the timing requirements for each device will be met.

The first step in the analysis is to draw timing diagrams that show the waveforms of the relevant signals with labels indicating the timing specifications. This may include signals generated by clocks, by the microprocessor, by memories and by interface circuits such as address decoders and buffers. Often there will be several timing diagrams for different parts of the circuit or for different sequences of signals. The timing diagrams are then used to derive expressions for the timing requirements of some devices in terms of the guaranteed timing responses of the other devices.

The expressions are derived by expressing the minimum (or possibly maximum) values of each requirement in terms of variables representing clock periods and other chip's timing guaranteed re-

sponses. When values are substituted for the variables in the equations a minimum (or possibly maximum) value is obtained for that requirement in that specific circuit. The difference between the computed requirement and the manufacturer's specified requirement is the *margin*. For example, if a manufacturer specifies that a certain flip-flop requires a 10 ns setup time and in a particular circuit the setup time is guaranteed to be at least 50 ns then the margin is 40 ns.

On the other hand, if any of the margins are negative then the chip's timing requirements are not met and the design must be changed. Typical changes include:

- adding CPU wait states
- latching signals to extend them
- using redundant logic gates to add small delays (poor practice)

Timing Diagrams

Timing diagrams help to clarify the meanings of timing specifications by labeling the times between signal transitions ("edges") using symbols from tables of timing specifications.

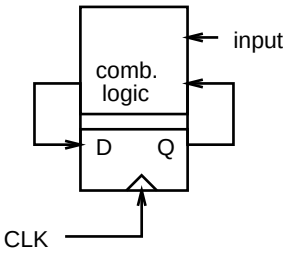
Some conventions used in timing diagrams are:

- high and low levels shown at the same time indicate the signal is fixed but can have either value (e.g. a data signal)
- shading between two levels indicates that the value is allowed to change during this time
- a single line between the two levels indicates that the signal is in high-impedance ("tri-state") state
- arrows drawn between transitions on different signals show that one signal transition causes or affects another
- sloped transitions between levels allow references to the signal reaching a low (V_{OL}/V_{IL}) or high (V_{OH}/V_{IH}) value

It is important to understand that timing diagrams are *not* drawn to scale. This allows chips with different specifications to share the same timing diagram, allows small delays to be shown more clearly and also allows the same label on the diagram to refer to both maximum and minimum values. Therefore you shouldn't necessarily rely on the timing diagram to show the order in which signal transitions happen.

Example

As a simple but complete example, consider a simple state machine where a combinational circuit computes the next state based on the current state and the input:



Exercise: Draw timing diagrams for the flip-flop and the combinational circuit.

Assume the flip-flops have a minimum setup time, t_s, of 20ns, a minimum hold time, t_h of 0 ns, that the maximum propagation delay through the combinational circuit is guaranteed to be $t_{PD} =$ 20 ns, and there is no minimum for t_{PD}. Assume the maximum clock-to-output propagation delay for the flip-flop is $t_{CO} = 5$ ns (again, with no minimum). Label the timing diagrams with each of these specifications.

Exercise: Draw a timing diagram for the complete circuit. It should include the clock CLK, the flip-flop's output, Q, and its input, D. Indicate cause–effect relationships between the signal edges using arrows.

Derive expressions for each timing requirement in terms of the clock period and guaranteed timing specifications for a clock frequency of 10 MHz. Substitute the actual values and compute the remaining margin. Will this circuit operate properly as far as timing is concerned? What if the hold time requirement was 5 ns?