THE UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ELEC 379 : Microcomputer System Design
1998/99 Winter Session Term 1

FINAL EXAMINATION
8:30 AM – 11:30 AM
December 7, 1998

This exam has four (4) questions. The marks for each question are as indicated. There are a total of 40 marks. Answer all questions. Write your answers in the exam book provided. Show your work. You may answer the questions in any order. Books, notes and calculators are allowed. You may keep this exam paper.

Question 1 (10 marks)

A defibrillator delivers shock(s) to a person experiencing a heart-attack to stop the heart-attack. This question asks you to design a controller for an automatic defibrillator.

The device has two one-bit active-high inputs: a `start` signal from a push-button switch and a `beat` signal from a heartbeat detector. The device has two one-bit active-high outputs: a `shock` signal which applies the shock when it is asserted and an `active` signal that turns on a warning LED to inform the operator that the device is active. The device also has a 1 kHz clock input.

The device has the following VHDL entity declaration:

```
library ieee ;
use ieee.std_logic_1164.all ;
use ieee.std_logic_arith.all ;

entity defib is
   port (
      start, beat, clk : in std_logic ;
      shock, active : out std_logic ) ;
end defib ;
```

When the device is first turned on it is "safe" and neither output is asserted.

After the operator has connected the electrodes, he/she pushes the `start` button momentarily and the device begins a two-second "listen" period. If the `beat` signal is asserted at any time within the two-second "listen" period then the device immediately reverts to the "safe" condition. If the two-second "listen" period expires before the `beat` signal is asserted, then the device asserts the `shock` signal for 1 millisecond and begins a new two-second "listen" period.

The `start` button has no effect unless the device is in a "safe" condition. The `beat` signal is ignored while the shock is being delivered. You may assume the `start` button will be pushed for more than 1ms.

The `active` output is asserted whenever the device is *not* in a "safe" condition.

Write an architecture that implements this device. Your design should be synthesizeable by MaxPlus+II. You need not include comments, `library` or `use` statements. You need not design the power-on reset circuit.

Hint: Select an appropriate number of states and draw a state transition diagram (and/or write the state transition table). Use "-" or "+".

Question 2 (10 marks)

Write a subroutine, `copyin:`, in 8086 assembly language that reads a string from an input port and stores it in a buffer `buf`. The parallel input port consists of an 8-bit data register at I/O (port) address 300H, and an 8-bit status register at I/O (port) address 301H. The status register has two one-bit status flags:

- bit 0 (the least-significant bit) is '1' only if there is an unread byte in the data register,
- bit 7 (the most-significant bit) is '1' only if there is an unread byte in the data register and there was a parity error while receiving the character in the data register.

and the other bits in the status register are always zero.

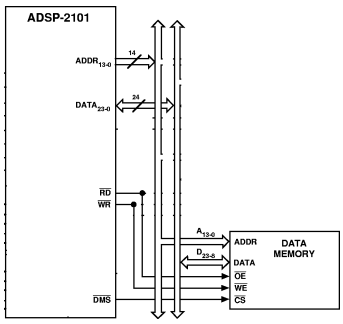
Your subroutine should copy all the characters from the I/O port the buffer. The copying should end when a null character (value 00H) is read. This null character should also be copied to the buffer. When your subroutine returns, it should set the value of AX to a non-zero value if *any* of the characters had parity errors in them, otherwise AX should be set to 0.

Your function must save and restore any registers it modifies (except AX, of course) before returning control to the calling function with a `RET` instruction. You must declare storage for any temporary variables you use. You may assume a buffer `buf` of the appropriate size has been declared elsewhere and is in the same data segment as used by your function. You need not include comments or assembler directives such as `segment`, `assume` or `org`.

Hints:

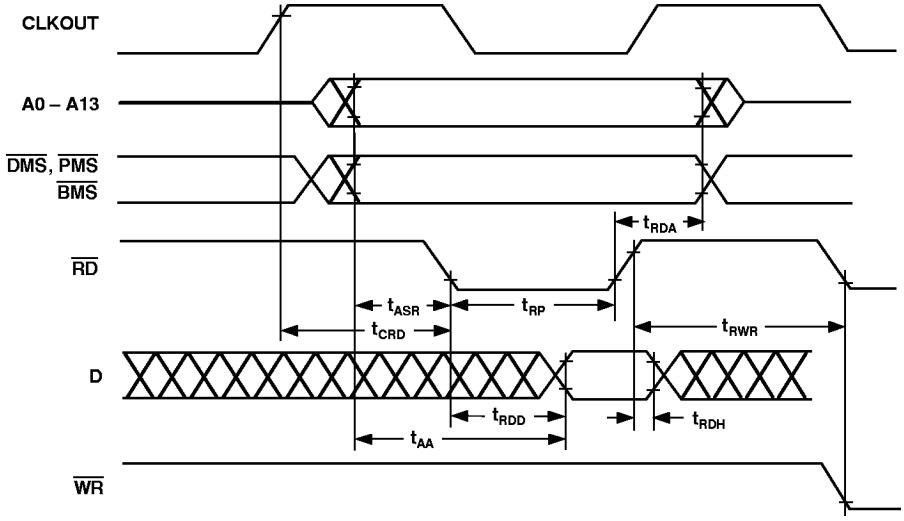
Question 3 (12 marks)

The following diagram shows the interface between an Analog Devices AD2101 DSP microprocessor and a Samsung KM62256D SRAM.



The microprocessor's $\overline{\text{DMS}}$ (data memory select) signal drives the RAM's chip select ($\overline{\text{CS}}$). The RAM's write enable ($\overline{\text{WE}}$) is driven by the CPU's write strobe ($\overline{\text{WR}}$) and the RAM's output enable ($\overline{\text{OE}}$) is driven by the CPU's read strobe ($\overline{\text{RD}}$). The RAM's address and data buses are connected to the corresponding CPU buses.

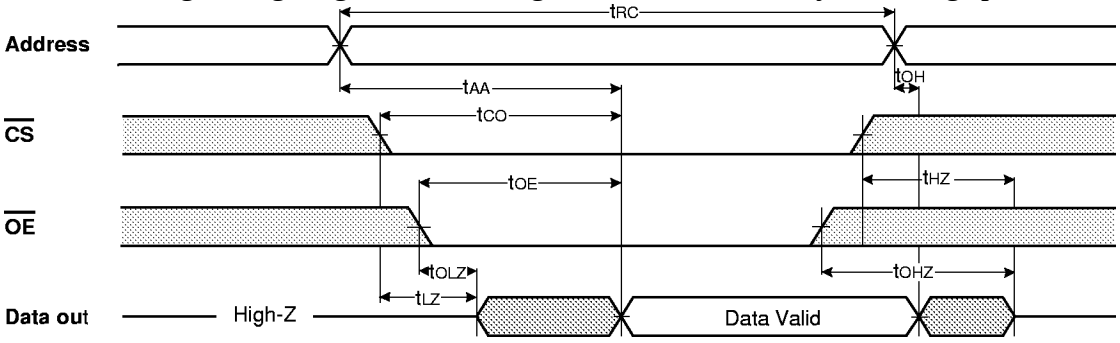
The following timing diagram and table provide the CPU's read-cycle timing specifications.



Characteristic	Symbol	Min	Max	Unit
$\overline{\text{RD}}$ Low to Data Valid	t_{RDD}		$0.5t_{\text{CK}} - 13 + w$	ns
A0–A13, $\overline{\text{DMS}}$ to Data Valid	t_{AA}		$0.75t_{\text{CK}} - 18 + w$	ns
Data Hold from $\overline{\text{RD}}$ High	t_{RDH}	0		ns
$\overline{\text{RD}}$ Pulse Width	t_{RP}	$0.5t_{\text{CK}} - 8 + w$		ns
A0–A13, $\overline{\text{DMS}}$ Setup before $\overline{\text{RD}}$ Low	t_{ASR}	$0.25t_{\text{CK}} - 10$		ns
A0–A13, $\overline{\text{DMS}}$ Hold before $\overline{\text{RD}}$ Deasserted	t_{RDA}	$0.25t_{\text{CK}} - 9$		ns
$\overline{\text{RD}}$ High to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	t_{RWR}	$0.5t_{\text{CK}} - 5$		ns
instruction cycle time		$t_{\text{CK}} + w$	$t_{\text{CK}} + w$	ns

where t_{CK} is the clock period and w is the number of wait states times t_{CK}. Assume $t_{\text{CK}} = 40$ns $w = 1 \times 40 = 40$ns.

The following timing diagram and table give the SRAM read-cycle timing specifications.



Characteristic	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	55		ns
Address access time	t_{AA}		55	ns
Chip select to output	t_{CO}		55	ns
Output enable to valid output	t_{OE}		25	ns
Output hold from address change	t_{OH}	10		ns

Determine which of the above timing specifications are Timing Requirements. Obtain expressions for these requirements in terms of Guaranteed Timing Responses. Obtain values for these expressions in nanoseconds. Find the amount by which each requirement is or is not exceeded (in nanoseconds) and state whether the requirement is met or not (Y[es] or N[o]). Summarize your answer in the form of a table as shown below.

Requirement		Guaranteed		Margin	Met
Symbol	Min. (ns)	Expression	Value	(ns)	(Y/N)
Read Cycle Requirements					

Question 5 (10 marks)

You need not justify your answers to the following questions. For multiple-choice questions choose the *best* answer. For True/False (T/F) questions write your answer as "True" or "False." For numeric questions show your calculations. Make sure your answer is unambiguous.

(a) Give the assembly language code that would force the execution of (and allow a return from) the standard interrupt service routine for the second serial port (serial port 2) on an IBM PC.

(b) Given a circuit with asynchronous inputs:

(i) We can avoid all metastability problems by registering all inputs. (T/F)

(ii) We can avoid all output glitches by registering all outputs (T/F).

(c) During the refresh interval a refresh circuit using CAS-before-RAS (CBR) refresh must generate addresses for:

(i) each row in a DRAM array

(ii) each column in a DRAM array

(iii) both (i) and (ii)

(iv) none of the above

(d) A register must be used to implement a parallel input port (T/F).

(e) An RS-232 serial interface is configured to send at 9600 bps, eight data bits and no parity. If characters are sent quickly as possible, exactly how long will it take to transmit 960 characters?

(f) To ensure reliable communications a DCE should always be connected to a DCE and a DTE should always be connected to a DTE (T/F).

(g) During a transfer of data from a peripheral to memory the 8237 DMA controller reads one byte at a time from the peripheral into its data register and then writes that byte to the memory (T/F).

(h) No CPU time is used by an interrupt-driven input interface while the device is not in use (T/F).

(i) In what direction does current flow when the output-enable of a tri-state output is not asserted (using standard conventions for current direction):

(i) into the output

(ii) out of the output

(iii) either (i) or (ii) depending on the output value

(iv) none of the above

(j) What minimum number of bytes must be left free on an application program's stack on an IBM PC to allow interrupts to execute and return properly? You may assume only one interrupt service routine will be active at any time.