Solution to Assignment 5
Timing Analysis

Question 1

Timing Specifications

You can use the following table to determine whether a timing specification is a guaranteed response or a requirement and the type of specification:

from	to	is always a
input	input	requirement width, setup, or hold time
input	output	response propagation delay
output	input	requirement width
output	output	response width

The assignment does not specify the operating voltage so you could have used either the 3V to 3.6V or the 2.7V to 3.6V specifications. I've assumed the supply voltage is above 3.0 volts and used the 25 MHz CLK specifications below even though CLK is actually CLK2$/2 = 12.5$ MHz.

Note that although some output-to-input minimum width specifications are labelled setup or hold requirements in the CPU specifications, the true setup/hold requirements are measured to an input signal, CLK2. These requirements appear in a earlier part of the table (e.g. t_{21} and t_{22}) and will be met if the "higher level" requirements given below are met.

From Lecture 5, Figure 1 a CPU cycle takes 4 CLK2 cycles or 160 ns if CLK2 is 25 MHz. This value should be used as the cycle time.

All times in nanoseconds.

In the tables below I've used the following abbreviations:

symbol	meaning
S	guaranteed timing response
R	timing requirement
C	CLK2 period (40 ns)
W_{min}	minimum width
W_{max}	maximum width
PD	propagation delay

Note that if the margin is zero the specification is met.

CPU Write Cycle

All the signals are outputs.

	R/S	type	value	from	to
t_{41}	S	W_{min}	0	address	WR*
t_{41a}	S	W_{min}	0	CS*	WR*
t_{42}	S	W_{min}	0	WR*	address
t_{42a}	S	W_{min}	0	CW*	CS*
t_{42b}	S	W_{min}	10	WR*	address
t_{43}	S	W_{min}	2C-10	data	WR*
t_{44}	S	W_{min}	C-10	WR*	data
t_{45}	S	W_{max}	C+10	WR*	data
t_{46}	S	W_{min}	2C-10	WR*	WR*

CPU Read Cycle

All signals except data bus are outputs.

	R/S	type	value	from	to
t_{47}	R	W_{max}	4C-41	address	data
t_{47a}	R	W_{max}	4C-42	CS*	data
t_{48}	R	W_{max}	3C-39	RD*	data
t_{49}	R	W_{min}	0	RD*	data
t_{50}	R	W_{max}	C	RD*	data
t_{51}	S	W_{min}	0	RD*	address
t_{51a}	S	W_{min}	0	RD*	CS*
t_{52}	S	W_{min}	3C-13	RD*	RD*

RAM Read Cycle

All signals except data bus are inputs.

	R/S	type	value	from	to
t_{RC}	R	W_{min}	70	address	address
t_{AA}	S	PD	70	address	data
t_{CO1}	S	PD	70	CE1*	data
t_{CO2}	S	PD	70	CE2	data
t_{OH}	S	PD	10	address	data
t_{LZ1}	S	PD	10	CE1*	data
t_{LZ2}	S	PD	10	CE2	data
t_{HZ1}	S	PD	30	CE1*	data
t_{HZ2}	S	PD	30	CE2	data

RAM Write Cycle

All signals are inputs except data bus for t_{WHZ} and t_{OW}). The RAM write cycle is WE* controlled (Chart 1) because the CPU timing specifications show that WE* (WR*) goes active after CE1* (CS1*).

	R/S	type	value	from	to
t_{WC}	R	W_{min}	70	address	address
t_{CW1}	R	W_{min}	50	CE1*	CE1*
t_{CW1}	R	W_{min}	60	CE2	CE2
t_{AW}	R	setup	50	address	WE*
t_{WP}	R	W_{min}	55	WE*	WE*
t_{DW}	R	setup	30	data	WE*
t_{DH}	R	hold	0	WE*	data
t_{AS}	R	W_{min}	0	address	WE*
t_{WR}	R	hold	0	WE*	address
t_{WHZ}	S	PD	30	WE*	data
t_{OW}	S	PD	10	WE*	data

Flash Read Cycle

All signals except data bus are inputs.

	R/S	type	value	from	to
t_{RC}	R	W_{min}	80	address	address
t_{ACE}	S	PD	80	CE*	data
t_{AOE}	S	PD	40	OE*	data
t_{AA}	S	PD	80	address	data
t_{OD}	S	PD	20	OE*, CE*	data
t_{OH}	S	PD	0	OE*, CE* address	data

Timing Analysis

We only need to verify that timing *requirements* are met.

CPU Requirements - RAM Read Cycle

Since RD* is not connected to the RAM, the CPU timing requirements relative to RD* cannot be checked.

	required	expression	margin
t_{47}	4C-41 = 119	t_{AA} = 70	49
t_{47a}	4C-42 = 118	t_{CO1} = 70	48
t_{48}	3C-39 = 81	unknown	
t_{49}	0	unknown	
t_{50}	C = 40	unknown	

CPU Requirements - Flash Read Cycle

	required	expression	margin
t_{47}	4C-41 = 119	t_{AA} = 80	39
t_{47a}	4C-42 = 118	t_{ACE} = 80	38
t_{48}	3C-39 = 81	t_{AOE} = 40	41
t_{49}	0	t_{OH} = 0	0
t_{50}	C = 40	t_{OD} = 20	20

RAM Requirements - CPU Read Cycle

	required	expression	margin
t_{RC}	70	4C = 160	90

RAM Requirements - CPU Write Cycle

	required	expression	margin
t_{WC}	70	4C = 160	90
t_{CW1}	50	$t_{41a} + t_{46}$ = 70	20
t_{CW2}	50		
t_{AW}	50	$t_{41} + t_{46}$ = 70	20
t_{WP}	55	t_{46} = 70	15
t_{DW}	30	t_{43} = 70	40
t_{DH}	0	t_{44} = 30	30
t_{AS}	0	t_{41} = 0	0
t_{WR}	0	t_{42} = 0	0

Flash Requirements - CPU Read Cycle

	required	expression	margin
t_{RC}	80	4C = 160	80