Solutions to Assignment 1
VHDL Synthesis

Question 1

The following solution attempts to reduce the complexity of the design by separating the counting and control functions. The four control inputs are combined into a three-bit operation-select value. This value is then used to select the next counter state.

The use of conditional assignmets would have simplified the description because of the prioritized operation of the reset and load controls but conditional assignments had not been covered in the lectures when this assignment was given out.

```
-- ELEC 379 Solution to Assignment 1
-- 74LS168 Decade Counter
-- Ed Casas, Sept 24 1998

entity sol1 is
port (
   sr, pe, cet, cep, cp : in bit ;
   p : in bit_vector (3 downto 0) ;
   q : out bit_vector (3 downto 0) ;
   tc : out bit ) ;
end sol1;

architecture rtl of sol1 is
   signal c, nextc, cplus1 : bit_vector (3 downto 0) ;
   signal operation : bit_vector (2 downto 0) ;
   signal countenable : bit ;
begin

   -- both cet and cep must be high to count
   countenable <= cet and cep ;

   -- build operation control word
   operation <= sr & pe & countenable ;

   -- operation selects source of next count
   with operation select nextc <=
        "0000" when "000",
        "0000" when "001",
        "0000" when "010",
        "0000" when "011",
        p      when "100",
        p      when "101",
        c      when "110",
        cplus1 when "111" ;

   -- next-count lookup table
   with c select cplus1 <=
        "0001" when "0000",
        "0010" when "0001",
        "0011" when "0010",
        "0100" when "0011",
        "0101" when "0100",
        "0110" when "0101",
        "0111" when "0110",
        "1000" when "0111",
        "1001" when "1000",
        "0000" when "1001",
        "1011" when "1010",
        "0100" when "1011",
        "1101" when "1100",
        "0100" when "1101",
        "1111" when "1110",
        "0000" when others ;

   -- connect count to output
   q <= c ;

   -- terminal count
   with c select tc <=
        cet when "1001",
        '0' when others ;

   -- instantiate the count register
   process(cp)
   begin
        if cp'event and cp = '1' then
                c <= nextc ;
        end if ;
   end process ;

end rtl ;
```

Figure 1 on page 2 shows the simulation output for the input conditions described in the assignment.

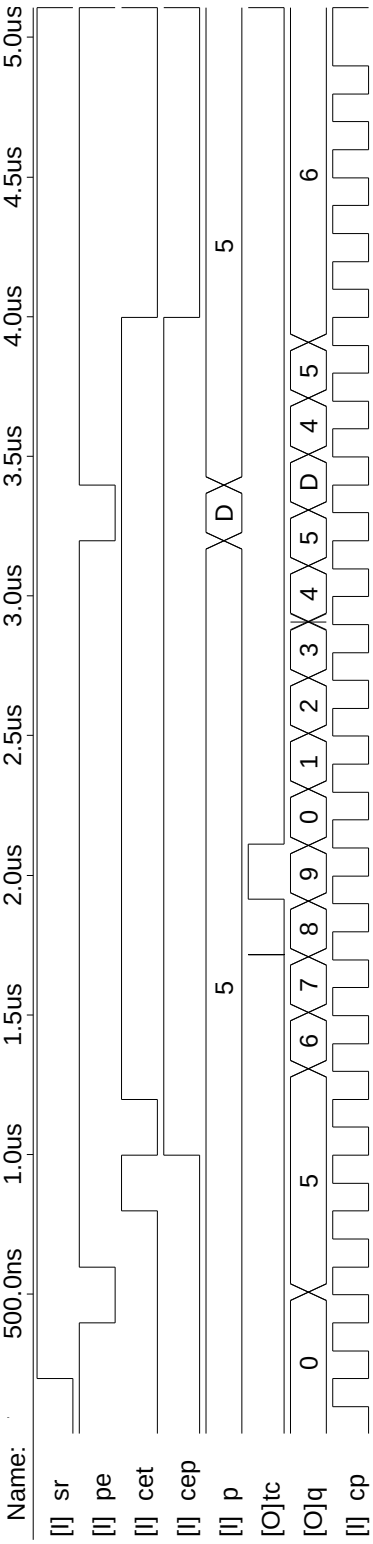

Figure 1: Simulation Waveforms