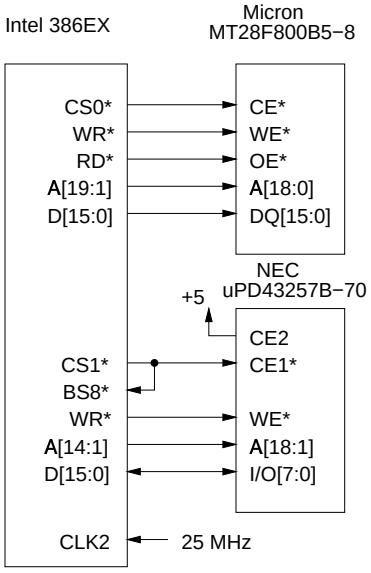
Assignment 5 - Timing Analysis

due
Friday, November 20, 1998
12:30 PM

Question 1

In this assignment you will perform a complete timing analysis on a simple microcomputer system. The design you are to analyze consists of: (1) an Intel 386EX microprocessor operating at 25 MHz, (2) an NEC μPD43257B-70 32k $\times$ 8 SRAM, and (3) a Micron MT28F800B5 512K $\times$ 16 'flash' EEPROM connected as follows:



The data sheets for these devices are available in PDF format at the following URLs. To do this assignment you'll only need to print out the pages containing the timing specifications and diagrams from each data sheet as shown below (you can, of course, print out more if you want to learn more about the devices).

- `ftp://download.intel.com/design/intarch/datashts/27242007.pdf` (Pages 38, 39 and 46).
- `http://www.ic.nec.co.jp/english/pdf/M10693EJ5V0DS00.pdf` (Pages 8, 9 and 10).
- `http://www.micron.com/flash/pdfs/q11.pdf` (Pages 4, 21 and 22).

The 386EX read and write cycles are the same as those of the 386SX. However, the 386EX (which is the chip used in the lab SBC) is designed to be used in control applications and several common peripherals have been integrated into the chip. These include six address decoders (the CSx outputs) and the logic for generating separate active-low read and write strobes (RD* and WR*).

From the timing diagram and your understanding of CPU bus cycles prepare a table identifying each CPU timing specification from t41 to t52 (inclusive) as a guaranteed response or a timing requirement. Also classify each specification as a propagation delay, setup time, hold time, maximum frequency, or a minimum width (choose the closest if none fit exactly). Repeat for the RAM read and write cycle specifications (pages 8 and 9) and for the flash read cycle specifications (page 21, omit the two specifications involving RP*).

Perform a timing analysis for three types of cycles: RAM read, RAM write and flash read (word). For each cycle, obtain an *equation* for each timing requirement as a function of the guaranteed responses and the clock periods (assume CLK2 is 25 MHz) and then compute the margin available for each requirement (negative if the requirement is not met). For each requirement that is not met, find the number of additional wait (T2) states that would have to be inserted so that the requirement would be met. Note any requirements where it is not possible to determine if the requirements are met.

Your results should be presented as four tables: one classifying the timing specifications and one for each timing analysis.