Assignment 1 - VHDL Synthesis

due
October 2, 1998
12:30 PM

Question 1

In this assignment you'll write a VHDL circuit description for an SN74LS162A decade counter.

Use your favourite Web browser to retrieve the data sheet for the SN74LS162A BCD decade counter from the Motorola Semiconductor Web server (the URL is given on the course page). The first two pages contain a functional description of the chip. Print out these two pages.

Write a VHDL entity statement for this device. Use the same signal names (e.g. `pe`, `p(0)`, `sr`, etc) as used in the data sheet. Use the `bit` type for the five control inputs and the `tc` output and use the `bit_vector` type with indices `(3 downto 0)` for `p` and `q`. Ignore power (Vcc) and ground. Use your initials plus the digits 162 as the entity name (e.g. if your name is Doug Mah, your entity statement would begin "`entity DM162 is` ...").

Write an architecture that models the behaviour of the device. Note that some of the inputs are active-low.

Include comments giving at least the purpose of the circuit ("decade counter"), the purpose of each major section of code, your name and student number, the course, and the date.

Use the Max+Plus II software to synthesize (compile) your design. Create test vectors (input waveforms) for your circuit that demonstrate the following behaviour of the device:

1. the output goes to zero when `sr` is asserted
2. if the `p` input is set to 5 and `pe` is asserted the output is set to 5
3. the output counts up only when both `cet` and `cep` are asserted
4. the output counts through all the legal values and "wraps around" back to 5
5. when the count is loaded with the value D (hex), the next count is 4.

Hand in a listing of your VHDL code and the simulator output (waveform editor window) showing correct behaviour.

Hints

VHDL does not allow an architecture to "read" (make use of) the value of an output port signal (e.g. `q`). You'll have to declare a signal internal to the architecture if you need to use an output value (e.g. for computing the next count value). This internal signal should then be "connected" (assigned) to the output port.

A straightforward implementation of a state machine using the four control signals and four counter state signals will require a $2^8 = 256$-entry lookup table to compute the next state. You almost certainly do not want to describe the circuit this way. One possible implementation is to encode the four control signals into a two-bit mode select signal corresponding to one of the four possible modes given in the table on the bottom of page 2. Other simplifications are possible.

Bonus marks will be awarded for the simplest solution that makes use of only those parts of VHDL that we have covered so far in the course.