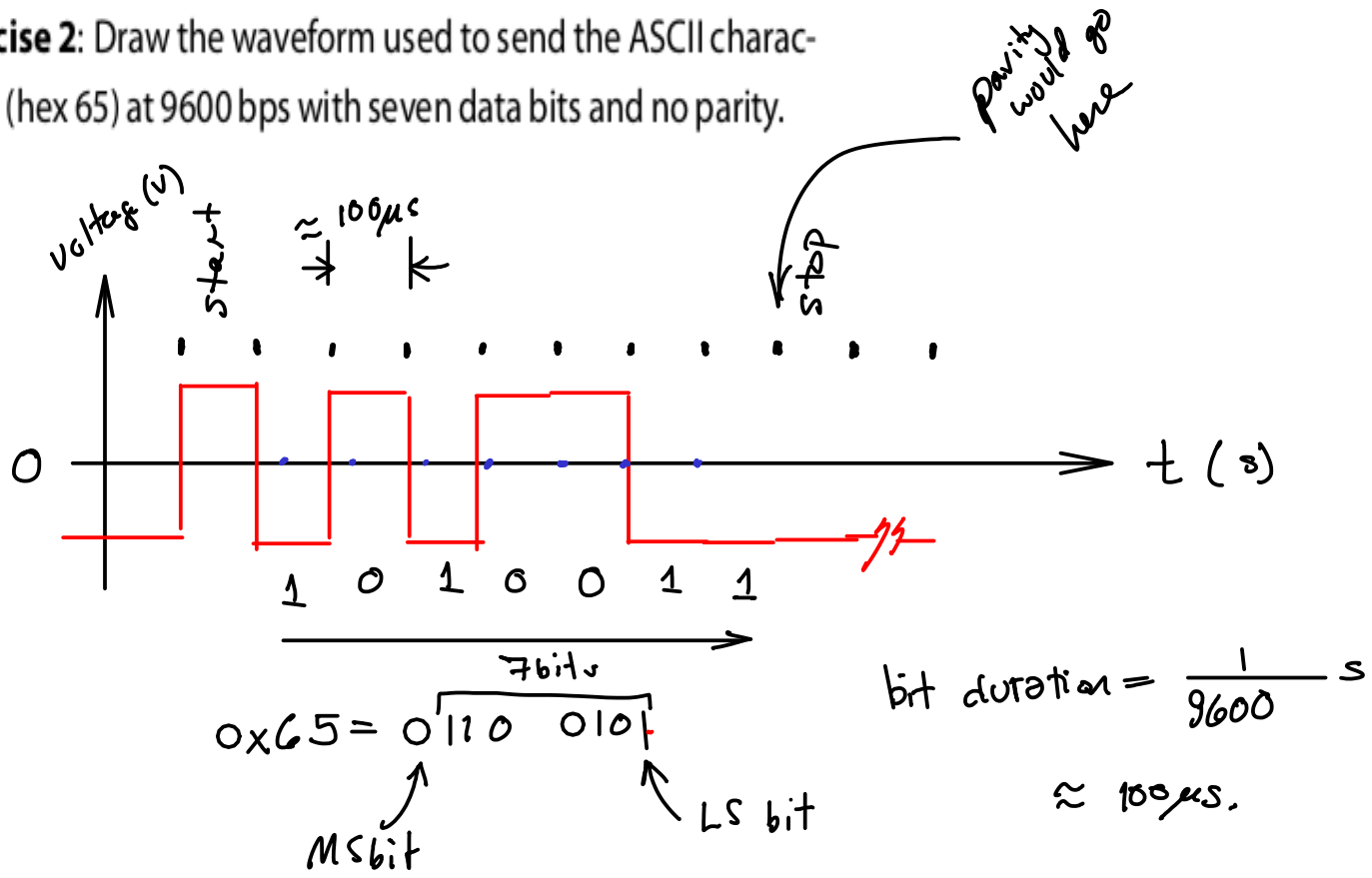
Lecture 4 - Asynchronous Serial Interfaces

Exercise 2: Draw the waveform used to send the ASCII character 'e' (hex 65) at 9600 bps with seven data bits and no parity.



Exercise 3: Will the parity bit allow the receiver to detect all single-bit errors? All double-bit errors?

yes

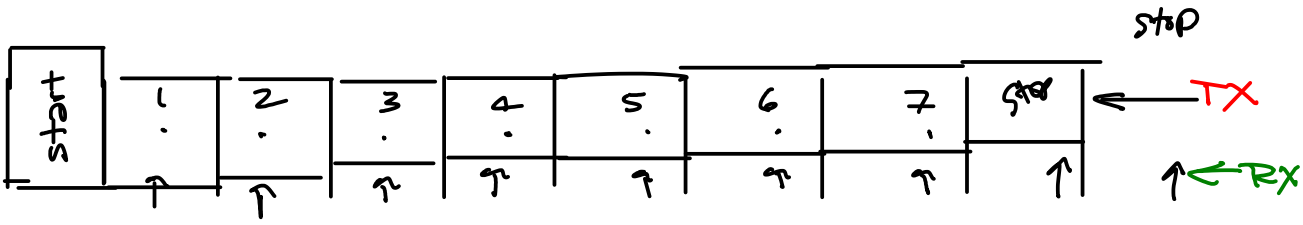
no

Exercise 4: What happens if the receiver's clock is running faster than the transmitter clock?

- receiver will sample earlier & earlier within the bit time
- if the clock error is sufficiently large it will sample the same bit twice & treat the MS bit as the stop bit (probably resulting in an error).

Exercise 5: What would happen if the receiver was expecting 8-bit characters and the transmitter was sending 7-bit characters? What about the reverse case?

⊕	0	1
0	0	1
1	1	0



→ receiver will see all bytes w/ MS bit = 1 and may see a "framing error" (the stop bit is H instead of L)

reverse case:

– if transmit M.S. bit = 0 (L) then receiver will see a H instead of stop bit (L) (Framing error).

Warning

0 bits = binary digits (for counting)

H voltages (measurable with DMM)

L

T truth values (indicate if an assertion is T or False)

F

these are three different things!

counter-examples:

$\overline{A0}$ = Ls bit of an address but H = 0, L = 1

$\overline{IRQ}$ = interrupt request?

but H = false
L = true