FEC and Convolutional Codes

Error Correcting Codes

Forward Error Correcting (FEC) are codes that include enough parity bits that the receiver can correct certain errors.

When the FEC code is well-matched to the error rate and to the types of errors likely to be encountered, the use of FEC results in higher throughput and better power efficiency.

Higher throughput results because blocks that contain correctable errors do not need to be retransmitted.

Exercise 1: If a rate-1/2 FEC code is used, what fraction of frames must contain correctable errors for the use of FEC to result in a net improvement in throughput?

Better power efficiency results if the same post-correction error rate can be achieved by transmitting less energy per information bit (E_b). This reduction in the required E_b to achieve a certain error rate is called the "coding gain".

Exercise 2: A system without coding needs to transmit at 1W to transmit 1 Mb/s at an error rate of 10^{-3}. When a rate-1/2 code is used the power to transmit the necessary 2Mb/s of data and parity bits decreases to 500mW. What is the channel bit rate in each case? What is the information rate in each case? What is E_b? What is the coding gain?

Although it is possible to use block codes to implement FEC, the trend until recently has been to use convolutional codes for communication systems. This was mainly because of the existence of a relatively simple and efficient decoding algorithm for convolutional codes called the Viterbi algorithm.

Convolutional Codes

A rate k/n convolutional code is implemented by reading a certain number of bits into a shift register and outputting a number of modulo-2 sums of these bits as shown below[1]

[1] Taken from the 802.11 standard.

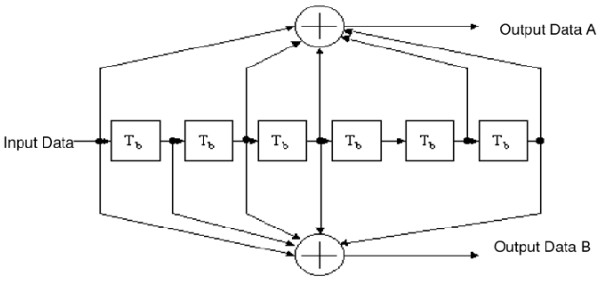

Figure 18-8—Convolutional encoder (k = 7)

If there are n output bits for each k input bits the rate of the code is k/n. The "constraint length," (K) of the code is the number of bits that can affect each output bit and is equal to the length of the shift register plus one (because the input bit is also used in computing the output).

Exercise 3: Assuming one bit at a time is input into the encoder in the diagram above, what are k, n, K and the code rate?

Viterbi Algorithm

Most FEC decoders use an algorithm called the Viterbi algorithm. This algorithm is a "maximum likelihood" decoder because it chooses the bit sequence with the minimum distance from the received sequence (or close to it).

The VA uses the trellis structure of the code to avoid exponential increase in decoding complexity with message length. Instead the complexity is proportional to 2^K where K is the constraint length. Although the algorithm is relatively complex, implementations are readily available as software, FPGA macros, synthesizable HDL and ICs.

Although many different convolutional codes are possible, there are certain standard codes that are used by many different systems. Hardware implementations are typically only available for these codes. The most common convolutional code is the rate-1/2 code with a constraint length of 7 shown above.

Higher-rate codes can be derived from the basic rate-1/2 code by not transmitting some of the bits. This is called "puncturing." The same decoder hardware can be used by feeding the decoder a value representing "unknown" (an "erasure") in place of the missing parity bits.

Exercise 4: Consider the encoder above. If the only the bits corresponding to the outputs A, A and B, and B are transmitted corresponding to every three input bits, what is the code rate of this punctured code?

Modern FEC Codes

Two other FEC codes have become popular in recent years because their error-correcting performance approaches the Shannon Limit.

Turbo Codes use two different codes to encode the data. The decoder uses the information from one code to help with decoding of the other code. Then that information is used to help decode the first code. The procedure is repeated iteratively until there are no errors (determined by a CRC) or a limit is reached.

Low Density Parity Check (LDPC) codes are block codes with sparse (few 1's) parity check matrices. This means that each parity bit is a function of only a few message bits.

Most FEC decoders use "soft-decision" decoding algorithms that operate on the probabilities that particular bits are zeros or ones rather than operating on binary "hard decisions".

Reed Solomon Codes

The Reed-Solomon code is a block FEC code that is widely used. RS codes operate on non-binary Galois fields, typically GF(256). It is able to correct a certain number of 8-bit word errors, regardless of the number of bit errors in each word. For this reason Reed-Solomon codes are efficient for channels that have bursty errors that cause multiple errors to fall within the same 8-bit word.