Lab 6 - Self-Synchronizing Descrambler

Modified May 1, 2013.

Introduction

In this lab you will design a self-synchronizing (multiplicative) descrambler using the Altera Quartus II FPGA design software and test it by simulating with a test waveforms supplied by the instructor.

The descrambler should multiply the input bits by the generator polynomial $G(x) = 1 + x^{-19} + x^{-21}$.

> The descrambler for this generator polynomial requires 21 flip-flops. If you prefer you may implemement a descrambler for the generator polynomial $G(x) = 1 + x^{-5} + x^{-9}$ which only requires 9 flip-flops. Simulation test waveforms will be supplied for both polynomials.
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> You may wish to refer to the description of the V.22 descrambler in lecture 14. The generator polynomial for the V.22 descrambler is $G(x) = x^0 + x^{-14} + x^{-17}$.

Procedure

Install the Quartus II software if it is not already installed. Install the software by running the Altera installer program available in the software folder in the course "share-out" drive. Supply the name of the folder in the same directory as the source of installation files. Select all of the defaults except that to minimize installation time the list of software to install should only include Quartus II Web Edition (Free), Quartus II Software (64-bit), and the MAX II device libraries.

Create a new project and a new block design file (BDF) using the block diagram editor. Add the components and I/O pins required. The descrambler should have three input pins (use the pin names resetN, clock and datain) and one output (dataout). The 'resetN' signal should set the state of the descrambler as if the previously received data was all-ones. The 'datain' and 'dataout' are the input and output data bits clocked on the rising edge of 'clock'. Save the project and design files and compile the design. If there are any errors, fix them and recompile the design.

Run the QSIM simulation program by running the command `quartus_sh --qsim` in the folder where the quartus_sh command is installed. Open the project and the waveform input file in the share-out folder. Run the simulation and show the simulation output to the instructor.

Report

The report should consist of your block diagram and the waveform .