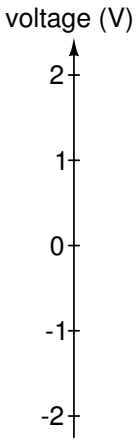
ELEX 3525 : Data Communications
2018 Fall Term

Assignment 2

Due Friday, November 9, 2018. Submit your assignment using the appropriate Assignment folder on the course web site. Assignments submitted after the solutions are made available will be given a mark of zero. **Show how you obtained your answers.**

Question 1

The diagram below shows the possible transmitted voltage levels (+2, +1, 0, -1 and -2 V) for a 5-level signalling scheme[1].



A signal of this type is received with added Gaussian noise that has a power of 150 mV_{rms}.

(a) What is the symbol error rate when a +1 V level is transmitted?

(b) What is the symbol error rate when a +2 V level is transmitted?

(c) If the answers are different, explain why.

Hints: Start by defining the decision threshold(s) and the range of noise voltage level(s) that would result in an error. You might find the problem easier to understand if you redraw the diagram horizontally.

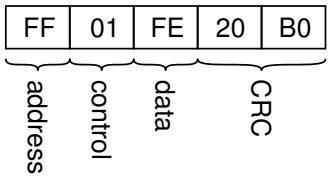
Question 2

The HDLC protocol defines a frame header and CRC error-checking in addition to the HDLC-style framing.

[1]For example, Gigabit Ethernet uses such a five-level signalling scheme.

The most common HDLC header is an 8-bit address field followed by an 8-bit control field.

Show the bits that would be transmitted (in binary notation), including the start and end flag sequences, for an HDLC frame with an address field of `0xff`, a control field of `0x01`, one byte of data with a value of `0xfe`, and a CRC of `0x20`, `0xB0`:



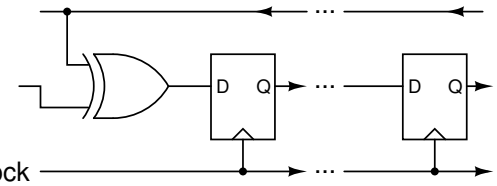
Please write out the bits for each transmitted byte on a separate line.

Question 3

Draw the schematic of a circuit that can divide a polynomial with coefficients from GF(2) by the generator polynomial:

$$G(x) = x^9 + x^4 + 1$$

The circuit consists of a sequence of flip-flops. The input to each flip-flop is either the output of the previous flip-flop (as in the stage on the right) or the output of the previous flip-flop xor'ed (added, in GF(2)) to another signal (as in the stage on the left):



Draw the appropriate number and types of stages required, and show (i) where the bits of the dividend polynomial are input (one bit per clock), and (ii) where the common input to the xor gates is connected.

Hint: Refer to the diagram in the lecture notes.