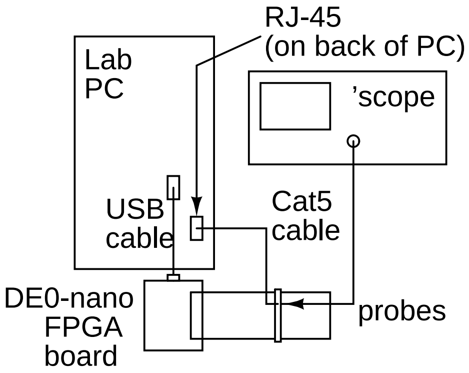
ELEX 3525 : Data Communications
2016 Fall Term

10 Mb/s Ethernet Transmitter

Introduction

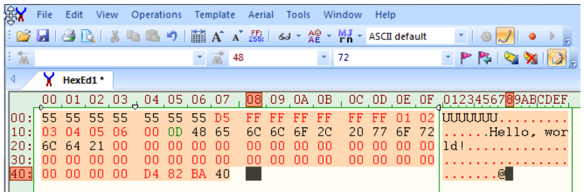
In this lab you will create an Ethernet frame using a hex editor and implement a simple interface to transmit that frame using the 10 Mb/s Ethernet PHY to a PC. You will use a 'scope to measure the interface voltages and signal timing. You will use the Wireshark protocol analyzer to display the frame contents.



Create An Ethernet Frame

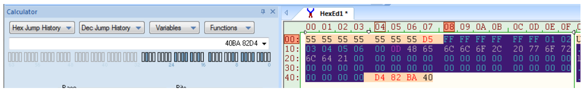
Run HexEdit and use menu item File⇒New to create a new file. Select a file size of 0 bytes. Right-click in the data area and select "Allow Changes". Use the Insert key to switch between inserting and over-writing existing values. Use the Tab key to switch between entering values as hex or ASCII characters.

Enter the bytes of an Ethernet packet that contains your full name as the data. Include the preamble and SFD. The destination address should be the broadcast address (all 0xff). The source address should be `1:2:3:4:5:6`. Set the length/type field to the length of the packet (although the value will be ignored by the hardware). The data field should contain your name padded with zeros if necessary to reach the minimum frame length.



```
     00 01 02 03  04 05 06 07  08 09 0A 0B  0C 0D 0E 0F  0123456789ABCDEF
00:  55 55 55 55  55 55 55 D5  FF FF FF FF  FF FF 01 02  UUUUUUU.........
10:  03 04 05 06  00 0D 48 65  6C 6C 6F 2C  20 77 6F 72  ......Hello, wor
20:  6C 64 21 00  00 00 00 00  00 00 00 00  00 00 00 00  ld!.............
30:  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00  ................
40:  00 00 00 00  D4 82 BA 40                            .......@
```

To compute the FCS, select the bytes *following the preamble* and compute the 32-bit CRC using the menu item Operation⇒Checksum⇒CRC 32. Add this 4-byte value to the end of the packet. Note that the CRC value computed by HexEdit is a 32-bit value that must be transmitted in order from LS to MS bit (i.e. you will have to reverse the byte order).



```
     00 01 02 03  04 05 06 07  08 09 0A 0B  0C 0D 0E 0F
00:  55 55 55 55  55 55 55 D5  FF FF FF FF  FF FF 01 02
10:  03 04 05 06  00 0D 48 65  6C 6C 6F 2C  20 77 6F 72
20:  6C 64 21 00  00 00 00 00  00 00 00 00  00 00 00 00
30:  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00
40:  00 00 00 00  D4 82 BA 40
```

Select all of the data (control-A) and export the packet contents to a file (e.g. `packet.hex`) in Intel hex format (File⇒Export⇒Intel Hex Records).

A Simple 10 Mb/s Ethernet Transmitter

A block diagram of the transmit side of a 10 Mb/s Ethernet transmitter is shown in Figure 1.

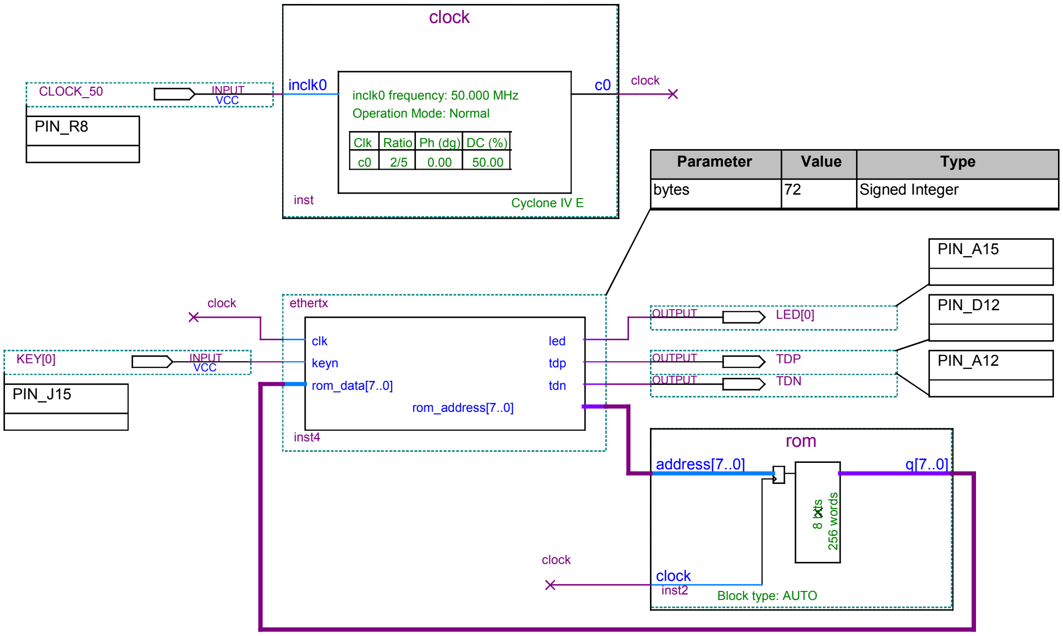
Most of the design is implemented in the `ethertx` module which is written in the Verilog hardware description language. The source is in the file ethertx.sv in the project archive if you're interested.

The two other blocks are a 20 MHz baud-rate clock and a ROM component to store the data to be transmitted.

Compile the Ethernet Transmitter

To use the supplied design files, download the `etherlab.qar` Quartus project archive file from the course web site and open it with Quartus Prime. Extract it to convenient folder (e.g. lab9). The project will then be opened.

Compile the design, program the FPGA and connect one side of the supplied ribbon cable to the

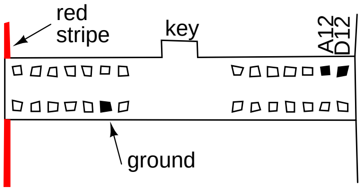


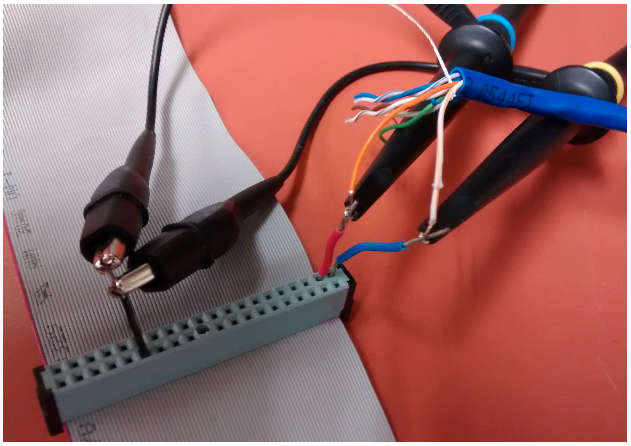
Parameter	Value	Type
bytes	72	Signed Integer

Figure 1: 10 Mb/s Ethernet Transmitter.

header pins on the side of the FPGA board that has the USB connector as in a previous lab.

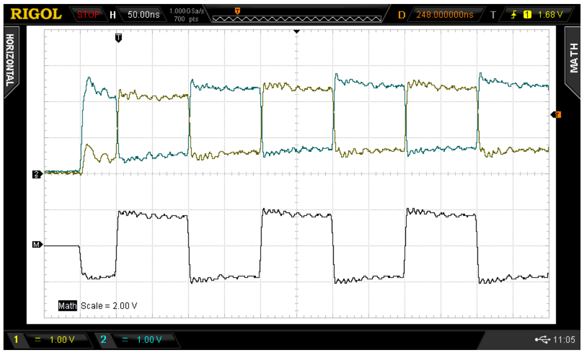
Use short wires to connect the two 'scope probes to the appropriate sockets on the other end of the ribbon cable and ground to the ground pin as shown below (you will connect the Cat-5 cable later):





Use the oscilloscope to check that the voltage levels, signal period and the preamble waveform are as expected. Do not connect either signal to ground! Use MATH mode (A-B) to measure the differential signal.

Set the 'scope trigger threshold at about 1.5 V. Reduce the sweep rate until one trace includes a complete frame then press RUN/STOP to hold the display. Use the horizontal position and scale knobs to view the start of the frame. Take a screen capture showing the superimposed ground-referenced signals and the differential voltage at the start of the packet:



Strip and connect the white/orange (RX+, pin D12) and orange (RX+, pin A12) wires at the other end of the cable. You can use the 'scope probes to connect these to the FPGA outputs as shown above.

Connect the Ethernet cable to the unused (lower) RJ-45 connector on the back of the PC. If necessary, ask the instructor for help in locating the right port.

Verify that the signal is not distorted. Unterminated cables reflect the signal back with a delay of ≈ 10 ns per meter of cable. This will cause ISI.

View Packets Using Wireshark

From the Start menu search for "View Network Connections". Find the network interface with the Realtek network interface card (NIC).

Run the Wireshark protocol analyzer. Select the network interface found above and click on "Start." Press the KEY0 button. The LED should light and you should now see packets being displayed that say "Hello world" in the data portion as shown in the screen capture below.

Edit the Data

Now that you have verified that the hardware works, you need to modify it to transmit the Ethernet frame you prepared in the Pre-Lab.

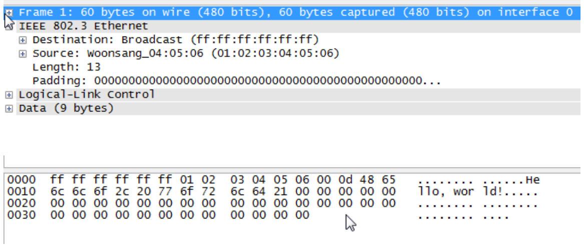
In the Project Navigator window's Files tab double-click the `.bdf` file to edit the schematic.

Depending on the size of your packet you may need to change the `bytes` parameter of the `ethertx` block. If so, double-click on the Parameter/Value/Type block and change the value in the "Parameter" tab. If you use a hex file name other than `testdata.hex` double-click on the ROM block and change the file name in the Mem Init tab.

After changing the name of the `.hex` file (or editing the contents of `testdata.hex`) and changing the packet length parameter if necessary, recompile the design, reprogram the FPGA and verify that the packets displayed by Wireshark include the desired data.

Show the instructor your packets being decoded to get marks for completing the lab.

Take a screen capture (or two) showing the contents of the 802.3 header and the complete contents of the packet in both hex and ASCII for your report. For example:



```
⊞ Frame 1: 60 bytes on wire (480 bits), 60 bytes captured (480 bits) on interface 0
⊟ IEEE 802.3 Ethernet
   ⊞ Destination: Broadcast (ff:ff:ff:ff:ff:ff)
   ⊞ Source: Woonsang_04:05:06 (01:02:03:04:05:06)
     Length: 13
     Padding: 000000000000000000000000000000000000000000000000...
⊞ Logical-Link Control
⊞ Data (9 bytes)

0000  ff ff ff ff ff ff 01 02  03 04 05 06 00 0d 48 65   ........ ......He
0010  6c 6c 6f 2c 20 77 6f 72  6c 64 21 00 00 00 00 00   llo, wor ld!.....
0020  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00   ........ ........
0030  00 00 00 00 00 00 00 00  00 00 00 00               ........ ....
```

Pre-Lab Report

Create the `.hex` file according to the instructions above. Submit a PDF file containing the usual identification information and a screen capture showing the contents of your packet including the CRC.

Bring the `.hex` file when you come to the lab.

Report

Submit a report including the following:

- the usual identification information
- a printout from HexEdit showing your packet's contents in hex and ASCII (including any corrections you made in the lab)
- a 'scope screen capture showing the single-ended and differential voltages at the start of the packet showing the preamble waveform
- screen captures from Wireshark showing the received Ethernet header and data fields.
- Answers to the following questions:

  (1) What is the minimum length of an 802.3 frame, not including the preamble? Does this include the header and FCS?

  (2) What is the frequency of the preamble waveform[1]? Why?

  (3) Assuming the minimum frame size, how many bytes will be transmitted per frame, including preamble and FCS?

  (4) What part(s) of the frame you created does Wireshark not show?

[1] Read the square wave's period from the 'scope screen capture and compute the frequency. The answer may not be what you expect.