

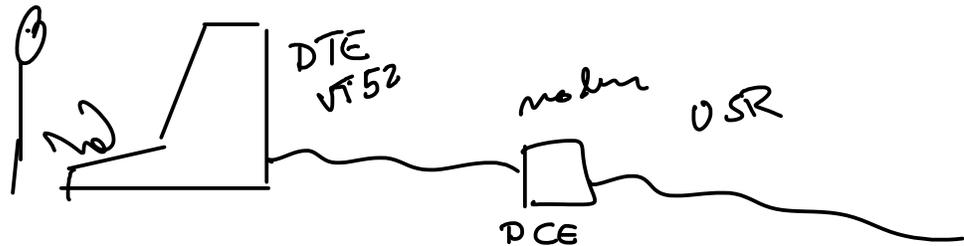
# Lecture 4 - Serial Interfaces

**Exercise 1:** Is the "Transmit Data" (TxD) signal an input or an output? How about "Receive Data" (RxD)? Is a computer a 'modem' or a 'terminal'?

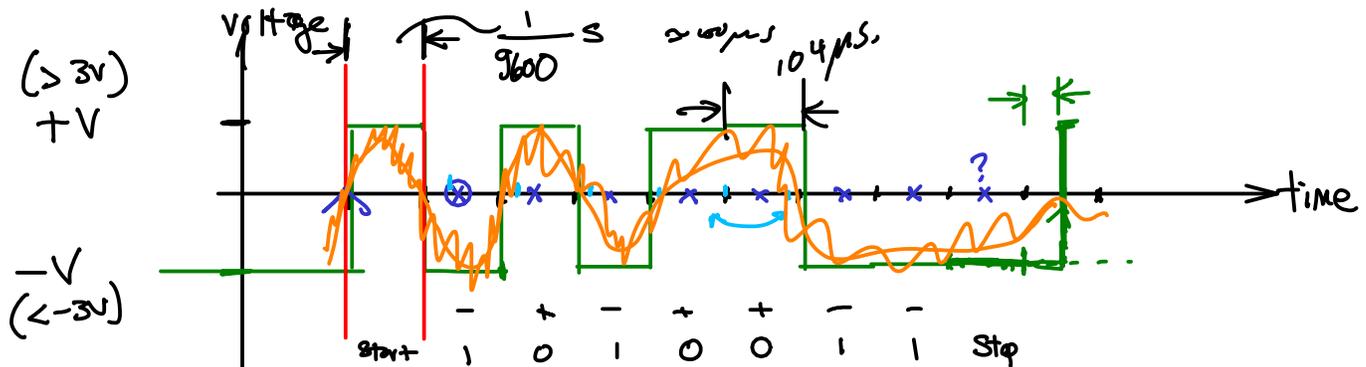
TxD is an input on a DCE (modem)  
 output on a DTE

RxD is input on DTE  
 output on DCE

PC are typically DTE  
 (minicomputer might be a DCE).



**Exercise 2:** Draw the waveform used to send the ASCII character 'e' (hex 65) at 9600 bps with seven data bits and no parity.



'e' = 0x65 = 01100101 (MS to LS)  
 = 1010011 (LS to MS, 7 bits)  
 = - + - + + - -

**Exercise 3:** Will the parity bit allow the receiver to detect all single-bit errors? All double-bit errors?

all single bit errors  $\rightarrow$  yes,  
any single bit error will change parity from even to odd or v-v.

all double-bit errors  $\rightarrow$  no

two inversions of parity result in same parity

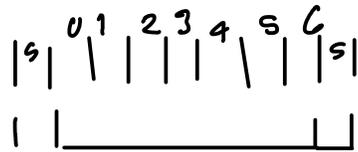
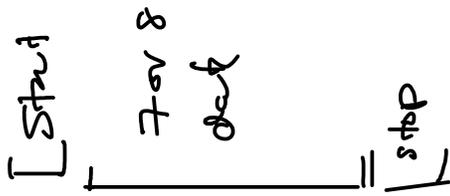
e.g. even  $\xrightarrow{\text{1st error}}$  odd  $\xrightarrow{\text{2nd error}}$  even

$P_e$	= prob. of 1 error	e.g.	1%
$(P_e)^2$	= prob of 2 errors		$10^{-4}$
$(P_e)^3$	= 3		$10^{-6}$

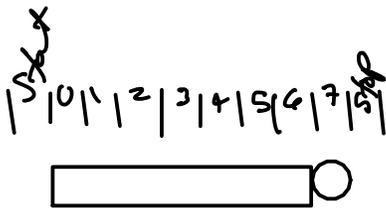
**Exercise 4:** What happens if the receiver's clock is running faster than the transmitter clock?

- receiver will sample too early  
- potentially may sample some bits twice

**Exercise 5:** What would happen if the receiver was expecting 8-bit characters and the transmitter was sending 7-bit characters? What about the reverse case?



→ receiver "picks up" the stop bit as the MS data bit & it is low = '1'



if MS bit was low (1) then is treated as extra stop bit

→ if MS bit was 0 (hi) receiver could notice wrong level for stop bit & declares a "framing" error.