Lecture 3 - Hierarchical Design in VHDL

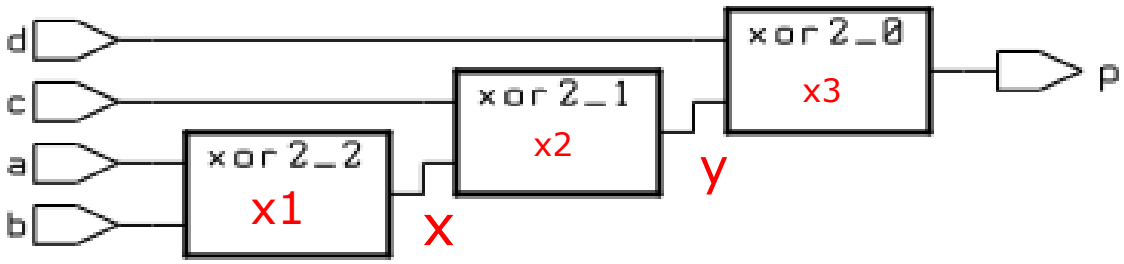
Exercise 1: Why is there no library statement in the second example?

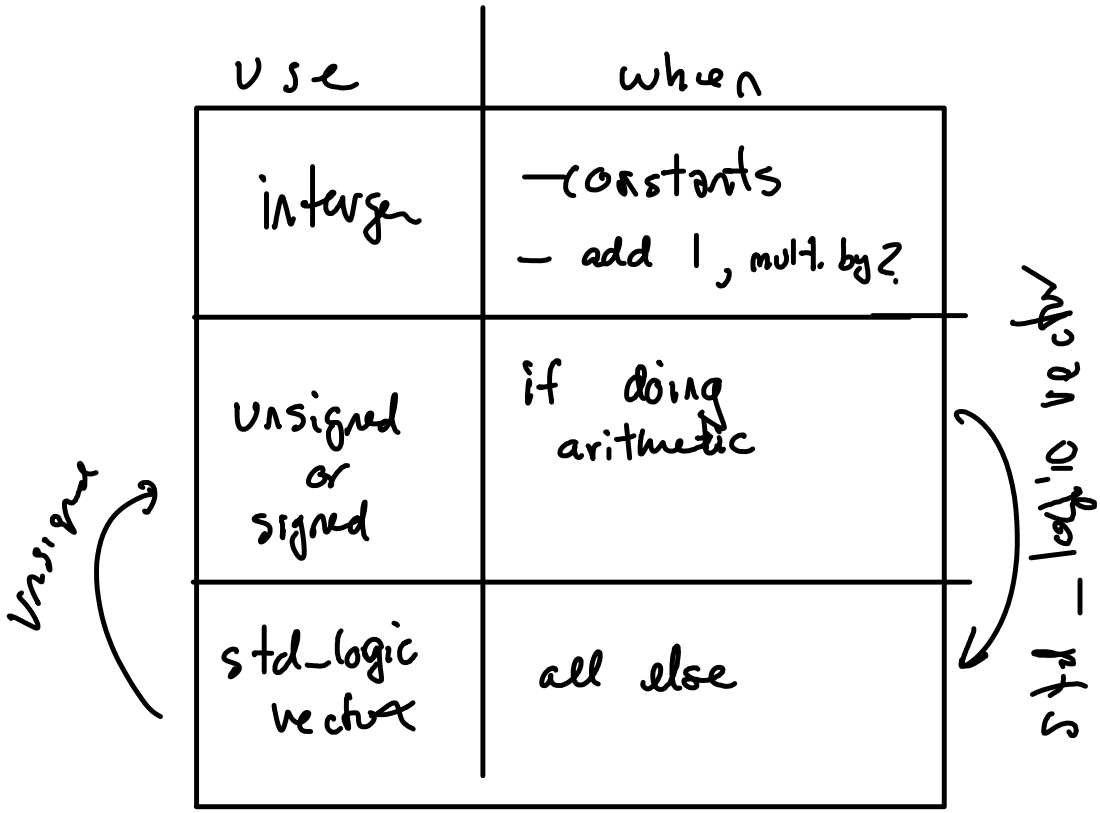
work library always ovailable.

Exercise 2: If this code was analyzed, what information would be saved? Where?

in library work
package flip flops
component rs
r, s inputs bit
q output bit

Exercise 3: Label the connections within the parity generator schematic with the signal names used in the architecture.





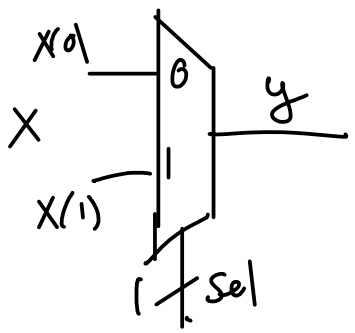
Exercise 4: (a) What is the type of the constant `X"1A_0002"`? (b) What is the purpose of the `to_unsigned()` function in the last line of the above example? (c) What conversion function(s) would you need to use if `r1addr` was declared to be of type `bit_vector`?

(a) X"1A_0002" → bit vector

(b) to_unsigned → to_unsigned() is the wrong function. The type of r1addr is std_logic_vector so the correct conversion function is unsigned().

(c) unsigned(to_stdlogicvector(r1adr))
(note that there are no underscores -- the names of the conversion functions are inconsistent and you will need to refer to the lecture notes, the quick-reference card or the IEEE 1164 library sources typically in c:\altera\15.0\quartus\libraries\vhdl\ieee\1993)

Exercise 5: Write a conditional assignment that models a 2-to-1 multiplexer. Use an array `x` as the input, a signal `sel` to select the input and a signal `y` as the output. Repeat for a 4-to-1 multiplexer (`sel` is now an array).



y <= X(0) when sel = '0' else X(1) ;