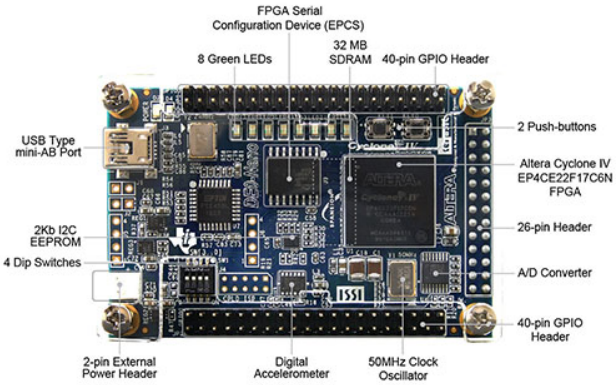
Combinational Logic Design with VHDL

Introduction

This lab introduces the use of VHDL for combinational logic design. You will design a circuit to display the last six digits of your student ID on an LED display.

You will design your circuit before coming to the lab. In the lab you will synthesize your design and program it into the FPGA on a DE-0 Nano board.

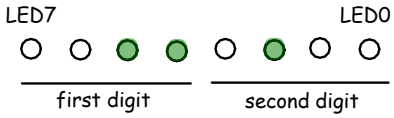
This board includes an Altera Cyclone IV FPGA, 8 LEDs labelled `LED7` through `LED0` and two push-buttons labelled `KEY1` and `KEY0`[1]:



Requirements

When neither button is pushed, the first two digits should be displayed in binary; if KEY0 is pushed, the second two digits should be displayed; if KEY1 is pushed the last two digits should be shown; if both buttons are pushed the behaviour is undefined.

Display the digits in binary-coded decimal format (BCD): the first digit on LED7 through LED4 and the second digit on LED3 through LED0. The most-significant bit should be on the left-most bit (LED7, LED3). For example, if your student ID was A00123456 and KEY0 was pushed then the display should show:



Note that the buttons are active-low and the LEDs are active-high. The DE0-Nano use manual is available on the course web site.

Pre-Lab

Write a VHDL entity and a synthesizable architecture that meets the requirements above. Your architecture may use selected assignment (multiplexer(s)) or `and`/`or` logic (sum of products).

Your design may contain errors since you will only be able to test it in the lab. However, it must be reasonably complete and synthesize without errors (see procedure below).

Submit a listing of your VHDL file to the appropriate dropbox on the course web site in PDF format along with the answers to the following questions for *your* design:

- which LEDs will be lit if neither button is pushed?
- which LEDs will be lit if both buttons are pushed?

FPGA Board

Do not make any connections to the FPGA board other than the USB cable. Failure to observe this rule will will result in a mark of zero for the lab.

The buttons are very small so you will need a pencil or small screwdriver to press them.

[1] Labelled photo from Terasic's DE0-Nano manual.

Lab Procedure

- start Quartus II or Quartus Prime
- select File > New > New Quartus II Project > OK
- create or select a folder, project name (e.g. `lab1`), an empty project with no files, the Cyclone IV E Family, the Specific device EP4CE22F17C6, and leave other settings set to defaults
- download `DE0_NanoX3330.qsf.zip` from the course web site and unzip the .qsf file into your project folder
- select Assignments > Import Assignments > `DE0_NanoX3330.qsf` to assign FPGA pin numbers to the signals on the DE0-Nano board
- select File > New... > VHDL File > OK
- enter your VHDL code and save it as *projectname*`.vhd`. Use *projectname* as the entity name. Declare the ports as `key: in (1 downto 0)` for the input and `led: out (7 downto 0)` for the output in order to match the names in the .qsf file.
- select Processing > Start Compilation (or press the icon). Correct any errors and recompile as necessary.
- connect the FPGA to the PC's USB port using the supplied cable
- select Tools > Programmer (or click on the icon)[2]
- if necessary, press Hardware Setup... and select USB-Blaster
- if necessary, press Add File... and select *projectname*`.sof` file in the `output_files` folder
- press Start to program the device
- check the operation of your circuit and fix any errors
- demonstrate your working circuit to the instructor to get credit for completing the lab

[2]To program the same file again, select `Chain1.cdf` in Project Navigator > Files.

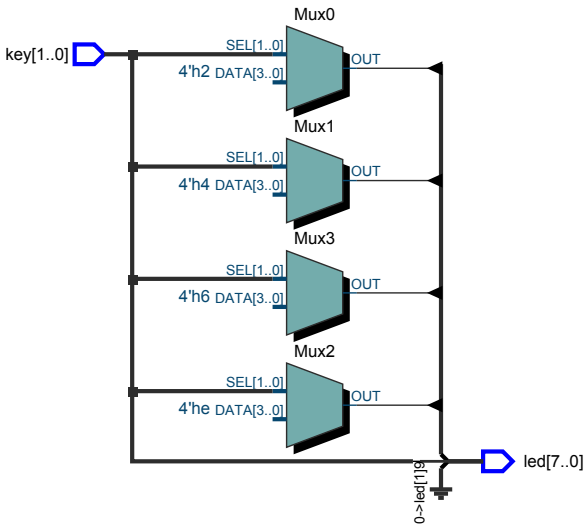
Lab Report

Submit a report in PDF format to the appropriate dropbox on the course web site containing the required identification information plus the following:

- your VHDL code with all errors corrected
- a screen capture of the Flow Summary section of the Compilation report showing the number of logic elements used. For example:

Flow Status	Successful - Tue Mar 29 00:13:27 2016
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Web Edition
Revision Name	lab1
Top-level Entity Name	lab1
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Final
Total logic elements	4 / 22,320 (< 1 %)
Total combinational functions	4 / 22,320 (< 1 %)
Dedicated logic registers	0 / 22,320 (0 %)
Total registers	0
Total pins	10 / 154 (6 %)

- the block diagram produced by running Tools > Netlist Viewers > RTL Viewer. For example:



Bonus marks may be awarded for the design that is the most concise (fewest statements), smallest (fewest logic elements) and clearest (easiest to understand).