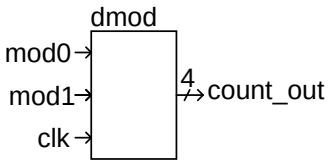
Solutions to Mid-Term Exam

Question 1

The following VHDL entity and architecture implement a resetable dual-modulo down-counter.




```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity dmod is
  port ( mod0, mod1, clk : in std_logic ;
         count_out : out unsigned(3 downto 0) ) ;
end dmod ;

architecture rtl of dmod is
  signal count, next_count : unsigned(3 downto 0);
begin

  next_count <=
    to_unsigned(0,count'length) when mod0 = '1' and
        mod1 = '1' else
    to_unsigned(3,count'length) when mod0 = '1' else
    to_unsigned(7,count'length) when mod1 = '1' else
    count - 1 ;

  process(clk)
  begin
    if clk'event and clk = '1' then
      count <= next_count ;
    end if ;
  end process ;

  count_out <= count ;

end rtl ;
```

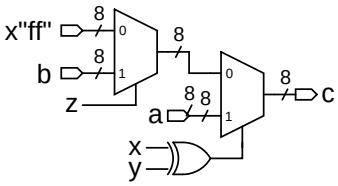
On the rising edge of `clk` the value of `count` is set to 0 if both `mod0` and `mod1` are active, otherwise to 3 if only mod0 is active, to 7 if only `mod1` is active, to or to `count`-1 otherwise. A second version of the question used values 5 and 10.

Question 2

The schematic corresponding to the following VHDL code:

```
c <=
  a when x /= y else
  x"FF" when z = '0' else
  b ;
```

is:



and the one corresponding to:

```
c <=
  x"00" when z = '0' else
  b when x /= y else
  a ;
```

is: