ELEX 3330 : Data Programmable Logic Devices
Term 201610

MID-TERM EXAMINATION
11:30 AM – 12:20 PM
April 3, 2016

Do not open this exam until you are told.

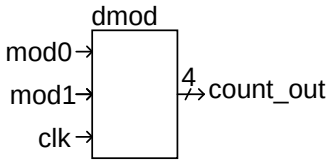
This exam is for:

Exam Version 0 A00123456

- *This exam has two (2) questions on four (4) pages. Answer all questions.*
- *The marks for each question are as indicated. There are a total of 12 marks.*
- *Write your answers and all rough work in this exam paper and nowhere else. Make a note if you continue your answer on the back of a sheet.*
- *Books and notes are allowed. No electronic devices other than calculators are allowed.*
- *Each exam is equally difficult. Answer your own exam.*

Question 1 (8 marks)

Write the VHDL entity and architecture for a resetable dual-modulo down-counter called `dmod`. The counter has a `clk` input and two active-high inputs `mod0`, and `mod1`. The counter has a 4-bit output called `count_out`.



The inputs should be declared `std_logic` and the output should be declared `unsigned`. Do not use `bit` or `bit_vector` types.

On the rising edge of `clk` the value of `count` should be set to 0 if both `mod0` and `mod1` are active, otherwise to 5 if only `mod0` is active, to 10 if only `mod1` is active, to or to `count`-1 otherwise.

Follow the course restrictions on `process()` statements (briefly: a process may include only simple assignments inside one if statement that tests only for a rising clock edge).

Question 2 (4 marks)

Draw the schematic corresponding to the following VHDL code:

```
c <=
  x"00" when z = '0' else
  b when x /= y else
  a ;
```

where x, y and z are single-bit inputs and a, b and c are 8 bits wide. Label all signals (input, output or connecting) with their names. Use conventional schematic symbols. Draw conditional assignments using multiple **two-input** multiplexers. Label each multiplexer input with the corresponding value of the select input. Show the bus widths for multi-bit signals.

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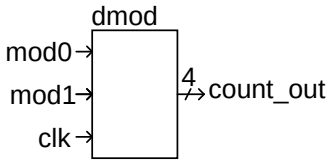

The inputs should be declared `std_logic` and the output should be declared `unsigned`. Do not use `bit` or `bit_vector` types.

On the rising edge of `clk` the value of `count` should be set to 0 if both `mod0` and `mod1` are active, otherwise to 3 if only `mod0` is active, to 7 if only `mod1` is active, to or to `count-1` otherwise.

Follow the course restrictions on `process()` statements (briefly: a process may include only simple assignments inside one if statement that tests only for a rising clock edge).

Question 2 (4 marks)

Draw the schematic corresponding to the following VHDL code:

```
c <=
  a when x /= y else
  x"FF" when z = '0' else
  b ;
```

where x, y and z are single-bit inputs and a, b and c are 8 bits wide. Label all signals (input, output or connecting) with their names. Use conventional schematic symbols. Draw conditional assignments using multiple **two-input** multiplexers. Label each multiplexer input with the corresponding value of the select input. Show the bus widths for multi-bit signals.