ELEX 3330 : Programmable Logic Devices
Term 201610

FINAL EXAMINATION (DRC VERSION)
12:30 – 4:30 PM
May 24, 2016

Do not open this exam until you are told.

This exam is for:

Exam Version 3 A00123456

- *This exam has three (3) questions on six (6) pages. Answer all questions.*
- *The marks for each question are as indicated. There are a total of 24 marks.*
- *Write your answers and all rough work in this exam paper* **and nowhere else**. *Make a note if you continue your answer on the back of a sheet.*
- *Books and notes are allowed. No electronic devices other than calculators are allowed.*
- **You may not leave the exam area until after 4:30 PM. You may not use any electronic equipment other than a calculator until after leaving the exam area. Violation of this instruction will result in a failing mark for the course.**

Name: _____

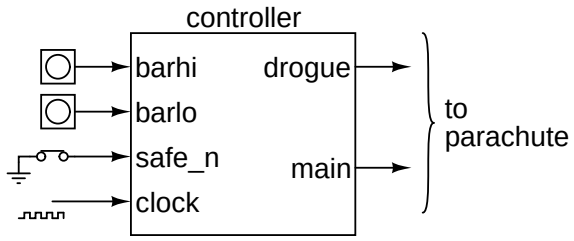
BCIT ID: _____

Signature: _____

Question	Mark
1	/10
2	/8
3	/6
Total	/24

Question 1 (10 marks)

This question asks you to design a controller that automatically opens a parachute.



The controller has two active-high altitude-detection inputs `barhi` and `barlo`, an active-low safety switch `safe_n` and a `clock` input. `barhi` is asserted at 500 m altitute or less. `barlo` is asserted at 100 m or less. `safe_n` is de-asserted when the parachute leaves the plane. `clock` is a one-pulse-per-second clock.

The controller has two active-high outputs: `drogue` and `main`. Both outputs should be set low whenever `safe_n` is asserted. Otherwise `drogue` should be asserted when `barhi` or `barlo` are asserted. `main` should be asserted 5 seconds after `drogue` is asserted or if `barlo` is asserted.

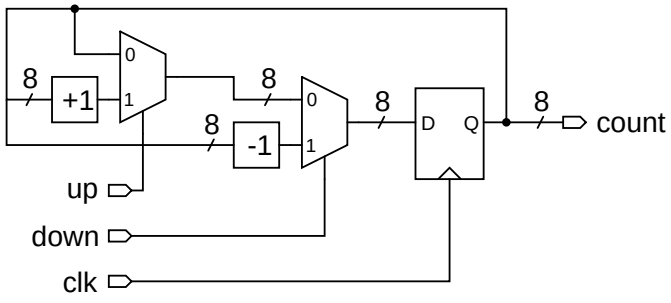
(a) Write the VHDL entity declaration for the controller called `controller`.

(b) Write a VHDL architecture that implements the controller.

Use `std_logic` and `unsigned` types only. You do not need to include `library` and `use` statements. You do not need to register the outputs.

Question 2 (8 marks)

Write a VHDL entity and architecture corresponding to the following schematic:



Use `std_logic` for single-bit signals (those where the bus width is not shown) and `unsigned` for multi-bit signals. Blocks labelled +/-1 add/subtract one from their inputs. Signals labelled in the schematic are entity inputs or outputs. You may choose any name(s) for signals within the architecture.

Question 3 (6 marks)

Draw the schematic corresponding to the following VHDL code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

architecture behav of exam is
   signal wave, waven : unsigned (14 downto 0) ;
   signal set, up, tick : std_logic ;
begin

  waven <=
    to_unsigned(1234,15) when set = '1' else
    wave+2 when up = '1' else
    wave ;

  process(tick)
  begin
    if tick'event and tick = '1' then
       wave <= waven ;
    end if ;
  end process ;

end behav;
```

Label all signals with their names. Use conventional schematic symbols. Draw conditional assignments using multiple **two-input** multiplexers. Label each multiplexer input with the corresponding value of the select input. Show the bus widths for multi-bit signals.