Assignment 2

Due Tuesday, May 17. Show your work. Submit your assignment using the appropriate dropbox on the course web site. Assignments submitted after the solutions are made available will be given a mark of zero.

Note: Answers to any of the following questions must follow the course restrictions on writing VHDL. In particular, the restrictions on process statements and registering outputs (if applicable). Use `std_logic[_vector]` and `unsigned` types.

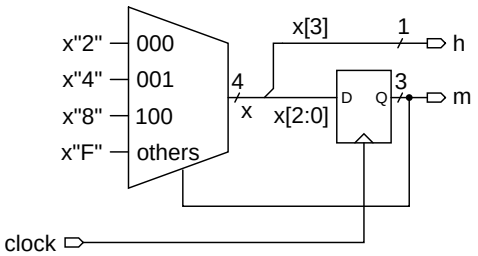
Question 1

Draw a schematic diagram for the following VHDL code. Label signals with the names used in the VHDL code. Use conventional schematic symbols for multiplexers, flip-flops and boolean operators. Use labelled blocks for VHDL arithmetic or comparison operators. Draw conditional assignments using multiple **two-input** multiplexers. Label each multiplexer input with the corresponding value of the select input. Show the bus widths on multi-bit signals.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
...
architecture rtl of asg2q4 is
  signal a, b : unsigned (2 downto 0) ;
  signal c, d : unsigned (7 downto 0) ;
  signal x, y, z : std_logic ;
begin

  with a select b <=
    "000" when "111",
    "111" when "000",
    "010" when others ;

  process(x)
  begin
    if x'event and x='1' then
      a <= b ;
      c <= d ;
    end if ;
  end process ;

  d <=
   to_unsigned(127,d'length) when y = '1' and z = '1' else
    to_unsigned(  0,d'length) when y /= z else
    to_unsigned(255,d'length) when c > 2 else
    to_unsigned(  1,d'length) ;

  y <= '1' when a < 5 else '0' ;

end rtl ;
```

Question 2

Write a VHDL entity and architecture for the following schematic:

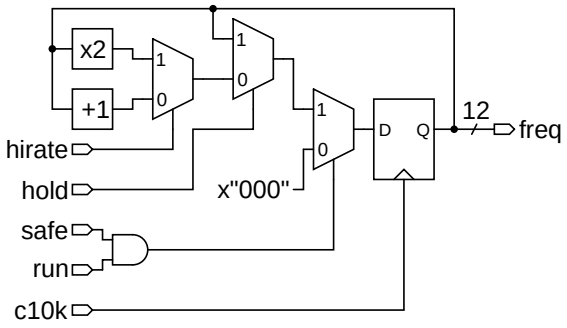


don't worry about whether the circuit does something useful (it doesn't) – just write the VHDL that would implement it. The numbers in brackets are ranges of subscripts (e.g. `x[2:0]` is `x(2 downto 0)`.

The inputs and outputs are denoted by the connector symbols (i.e. outputs are `h` and `m` and the input is `clock`).

Question 3

Write a VHDL entity and architecture for the following schematic:



All multiplexers are 12 bits wide.

Question 4

Write the VHDL entity and architecture for a controller that will "slow start" a motor. Your controller has two one-bit outputs: `on` and `fast` and three one-bit inputs `start`, `stop` and `speed`.

When the `start` input is high the `on` output should be set high until the `speed` input is high and then both `on` and `fast` should be set high. If at any time the `stop` input is high then both `on` and `fast` should be set to off. If `start` and `stop` are both low or both high then there should be no change in the outputs.

Question 5

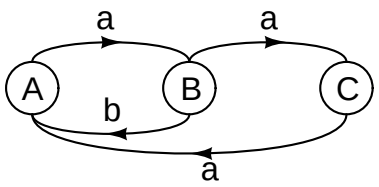
Write a VHDL entity and architecture for a circuit that has a 1 MHz clock input called `clk`, an active-low synchronous reset input `reset_n`, and an output called `pulse2` that is high for 2 μs once every 20 μs.

Question 6

Write the VHDL architecture for the entity:

```
entity controller is
  port ( en, f, clk : in std_logic ;
    G, Y : out std_logic ) ;
end controller ;
```

that implements a state machine with the following state transition diagram:



where the output `G` is 1 in states A and B and 0 otherwise and the output `Y` is 1 in state B and 0 otherwise. The transition condition *a* is that `en` is 1. The transition condition *b* is that `f` and `en` are both 1. The state remains the same for all other input conditions. State transitions happen on the rising edge of `clk`.