ELEX 2117 : Digital Techniques 2
2025 Winter Term

Quiz 2
9:30 AM – 10:20 AM
Thursday, January 20, 2024
SW09-110

This exam has two (2) questions on one (1) pages. The marks for each question are as indicated. There are a total of eight (8) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

0

ELEX 2117 Quiz 1 A00123456 0

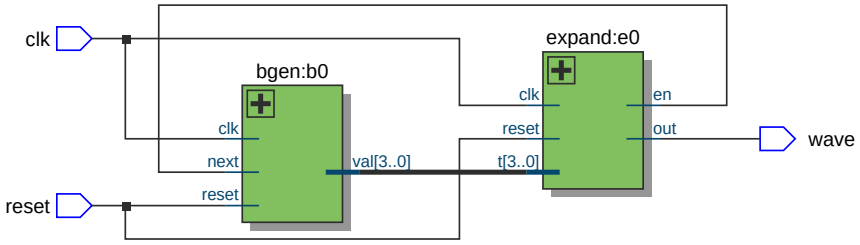
Question 1 — 4 marks

Given the following module declarations:

```
module bgen #(parameter b)
   ( input logic reset, clk, next,
     output logic [b-1:0] val ) ;

module expand #(parameter b)
   ( input logic reset, clk,
     input logic [b-1:0] t,
     output logic en,
     output logic out ) ;
```

Write a Verilog module named **`tgen`** that implements the following diagram:

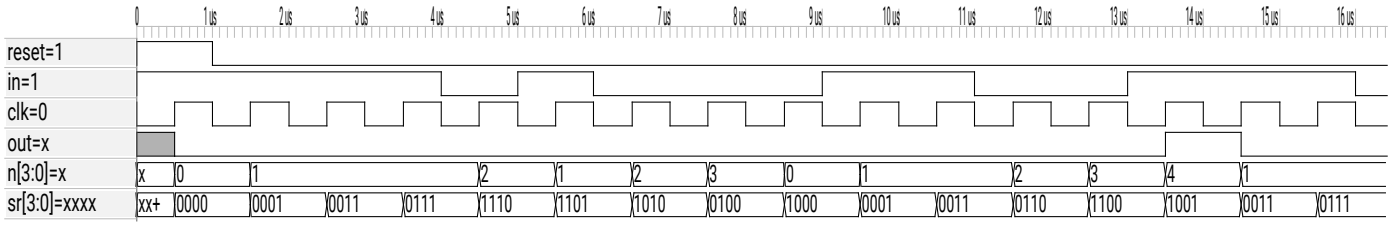


Declare any additional signals required to implement the diagram, using any valid signal names. Use a value of 4 for the parameter **`b`** in each instantiation. You may use any of the conventions for associating signals and ports.

Question 2 — 4 marks

Write a module named **`detect`** with one-bit inputs named **`clk`**, **`reset`**, and **`in`**, and a one-bit output named **`out`**.

`out` should be set to 1 when the sequence 1, 0, 0, 1 has appeared on **`in`** on consecutive rising edges of **`clk`**. When **`reset`** is asserted it should be assumed all previous and current values of **`in`** were/are 0. **`out`** should be set to 1 at the rising edge of **`clk`** on the last value of the sequence and stay high for one **`clk`** period. For example:



Any correct solution is acceptable. The timing diagram above shows two possible state variables that you could use. **`n`** counts the correct number of values seen; **`sr`** stores the most recent four input values.

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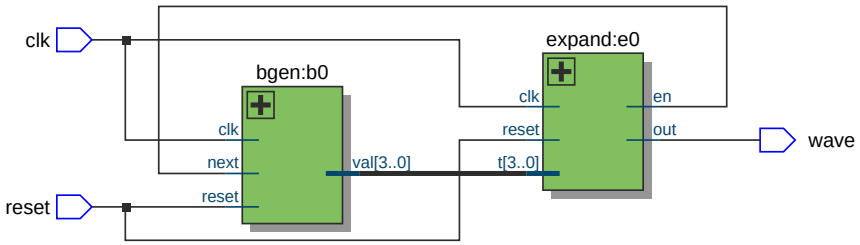

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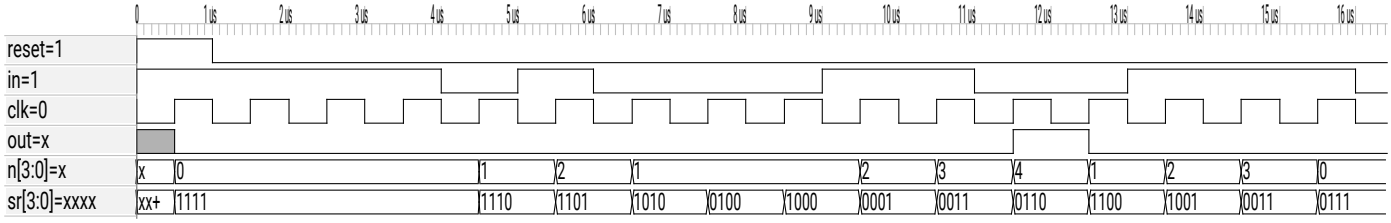
Write a module named **`detect`** with one-bit inputs named **`clk`**, **`reset`**, and **`in`**, and a one-bit output named **`out`**.

`out` should be set to 1 when the sequence 0, 1, 1, 0 has appeared on **`in`** on consecutive rising edges of **`clk`**. When **`reset`** is asserted it should be assumed all previous and current values of **`in`** were/are 1. **`out`** should be set to 1 at the rising edge of **`clk`** on the last value of the sequence and stay high for one **`clk`** period. For example:



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