ELEX 2117 : Digital Techniques 2
2025 Winter Term

Quiz 1
9:30 AM – 10:20 AM
Thursday, January 23, 2024
SW09-110

This exam has two (2) questions on one (1) pages. The marks for each question are as indicated. There are a total of ten (10) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

0

Question 1 — 6 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'hA6` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h6`
`x[5:4] || y ^ y`	
`1 >= 1 < 1`	
`y[3:2] | x`	
`{ y >> 4, x }`	
`y * ( y < x[7:4] )`	
`x[4] ? x[7] : !x[7] ? x[7:4] : x[7:0]`	

Question 2 — 4 marks

Write a Verilog module named `next` that has a 16-bit `logic` input named `cnt` and a 16-bit logic output named `cnt_next`. `cnt_next` should be set to 8190 if the value of `cnt` is less than or equal to zero otherwise it should be set to `cnt` minus three. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.

ELEX 2117 : Digital Techniques 2

2025 Winter Term

Quiz 1

9:30 AM – 10:20 AM

Thursday, January 23, 2024

SW09-110

This exam has two (2) questions on one (1) pages. The marks for each question are as indicated. There are a total of ten (10) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Paper, Test 2 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

Question 1 — 6 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

```
logic [7:0] x ;
logic [3:0] y ;
```

and that `x` has the value `8'h38` and that `y` has the value `4'b0101`. The first row has been filled in as an example. You need not show your work or draw another box around the answer

expression	value
`x[3:0]`	`4'h8`
`x[5:4] && y ^ y`	
`1 > 1 < 1`	
`x[5:4] & y`	
`{ y >> 4, x }`	
`y * ( y > x[7:4] )`	
`x[4] ? x[7] : !x[7] ? x[7:4] : x[7:0]`	

Question 2 — 4 marks

Write a Verilog module named `next` that has a 16-bit `logic` input named `cnt` and a 16-bit logic output named `cnt_next`. `cnt_next` should be set to zero if the value of `cnt` is greater than or equal to 4095 otherwise it should be set to `cnt` plus one. Declare arrays in decreasing bit order. Follow the course coding guidelines but omit comments.