ELEX 2117 : Digital Techniques 2
2025 Winter Term

MIDTERM EXAM 2
2:30 PM –
Wednesday, March 5, 2025
SW01-1205

This exam has four (4) questions on two (2) pages. The marks for each question are as indicated. There are a total of nineteen (19) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

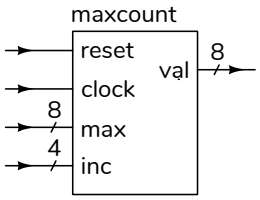
BCIT ID: _____

Signature: _____

0

Question 1 — 3 marks

Write a Verilog module named **`maxcount`** with logic inputs named **`reset`** and **`clock`**, an 8-bit logic array input named **`max`**, a 4-bit logic array input named **`inc`**, and an 8-bit logic array output named **`val`**.



The output only changes on the rising edge of **`clock`**. If **`reset`** is asserted or **`val`** is equal to zero then **`val`** is set to **`max`**, otherwise **`val`** is decremented by **`inc`**. Follow the course coding guidelines but omit comments.

Question 2 — 6 marks

Write a Verilog testbench module named **`maxcount_tb`** that:

- declares any necessary variables
- instantiates the module **`maxcount`** described in the previous question
- sets **`max`** to a value equal to the last two digits of your BCIT ID and **`inc`** to 4
- creates a continuous 10 MHz clock, starting with a low (0) value
- asserts reset for exactly one clock cycle
- terminates (rather than pauses) the simulation when **`val`** is equal to **`0`**

You need not include comments or create a **`.vcd`** file.

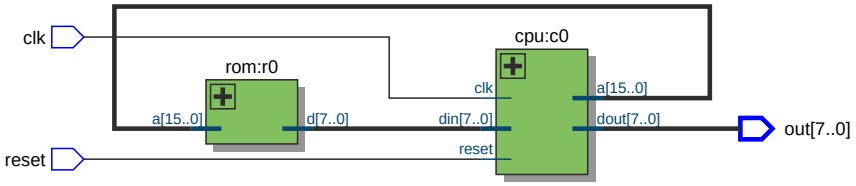
Question 3 — 4 marks

Given the following module declarations:

```
module rom #(parameter b, w)
   ( input logic [w-1:0] a,
     output logic [b-1:0] d ) ;
```

```
module cpu #(parameter b, w)
   ( input logic clk, reset,
     input logic [b-1:0] din,
     output logic [b-1:0] dout,
     output logic [w-1:0] a ) ;
```

Write a Verilog module named **`system`** that implements the following diagram:



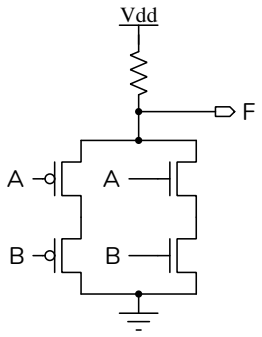
Declare any additional signals required to implement the diagram, using any valid signal names. Use a value of 8 for the parameter **`b`** and a value of 16 for the parameter **`w`** in each instantiation. Use explicit port and parameter names (e.g. **`.port(signal)`**, **`.port`**, or **`#(.parameter(`*n*`))`**).

Question 4 — 6 marks

(a) The following table shows the voltages on inputs A and B for the circuit shown below. H corresponds to a voltage above the gate threshold voltage and L corresponds to 0 V.

Fill in the last column of the table with the voltage at point F of the circuit. Use H for a voltage of approximately V_{dd} and L for a voltage of approximately 0 V.

A	B	F
L	L	
L	H	
H	L	
H	H	



(b) An IC has specifications of $V_{\mathtt{IL}} = 0.3\,\mathrm{V}$ and $V_{\mathtt{IH}} = 0.7\,\mathrm{V}$. If you needed a noise margin of 0.2 V for both high and low voltages, what are the required maximum $V_{\mathtt{OL}}$ and minimum $V_{\mathtt{OH}}$?

(c) A circuit draws 200 mA when operating with a clock frequency of 50 MHz. You would like to operate this circuit for a year when powered by a CR2016 battery that has a capacity of 100 mAh. What clock frequency should you use? *Hints: $P = IV$. V does not change. There are $365 \times 24 = 8760$ hours in a year.*

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Sample Exam 2 A01234567

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Name: _____

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255

Question 1 — 3 marks

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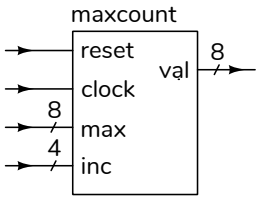

The output only changes on the rising edge of **`clock`**. If **`reset`** is asserted or **`val`** is equal to **`max`** then then **`val`** is set to zero, otherwise **`val`** is incremented by **`inc`**. Follow the course coding guidelines but omit comments.

Question 2 — 6 marks

Write a Verilog testbench module named **`maxcount_tb`** that:

- declares any necessary variables
- instantiates the module **`maxcount`** described in the previous question
- sets **`max`** to a value equal to the last two digits of your BCIT ID and **`inc`** to 2
- creates a continuous 50 MHz clock, starting with a low (0) value
- asserts reset for exactly one clock cycle
- terminates (rather than pauses) the simulation when **`val`** is equal to **`max`**

You need not include comments or create a **`.vcd`** file.

Question 3 — 4 marks

Given the following module declarations:

```
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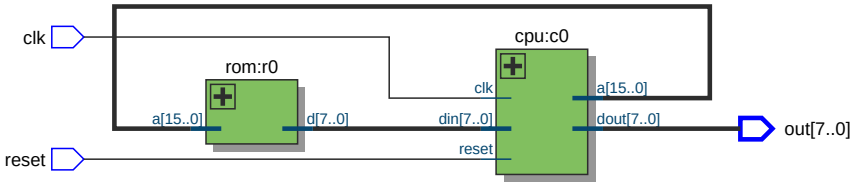

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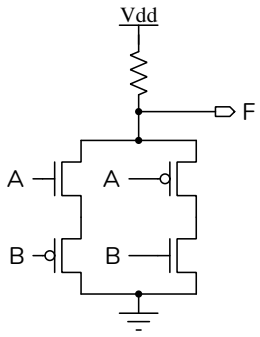
H	L	
H	H	



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(c) A circuit draws 50 mA when operating with a clock frequency of 50 MHz. You would like to operate this circuit for a year when powered by a CR2016 battery that has a capacity of 100 mAh. What clock frequency should you use? *Hints: $P = IV$. V does not change. There are $365 \times 24 = 8760$ hours in a year.*