ELEX 2117 : Digital Techniques 2
2025 Winter Term

MIDTERM EXAM 1
10:30-12:20
Wednesday, February 5, 2025
SW01-1021

This exam has three (3) questions on four (4) pages. The marks for each question are as indicated. There are a total of twelve (12) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Underline or draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. **Show your work.**

This exam paper is for:

Sample Exam 1 A00123456

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 3 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

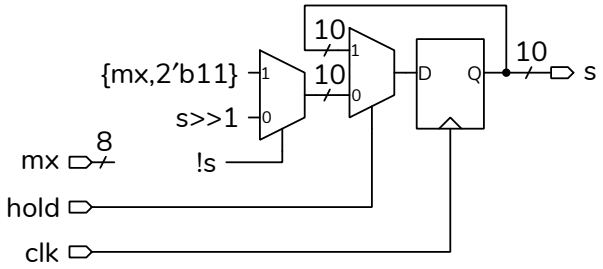
```
logic [3:0] x ;
logic [7:0] y ;
```

and that `x` has the value `4'b0110` and that `y` has the value `8'h5A`. The first row has been filled in as an example. You need not show your work or draw another box around the answer.

expression	value
`y[3:0]`	`4'hA`
`y[5:0] + x * x`	
`x && ! ( 8 & y ) ^ 1`	
`~ y & 1 ? ~ ( y & 1 ) ? 0 : 1 : 2`	

Question 2 — 5 marks

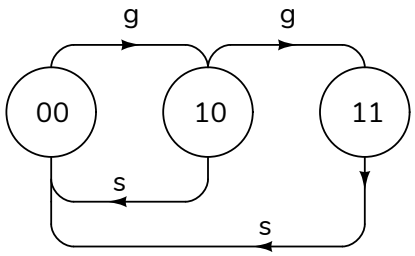
Write a Verilog module named **`ctrl`** that implements the following block diagram. The diagram follows the course conventions for block diagrams. Follow the course coding guidelines but omit comments.



Question 3 — 4 marks

A state machine with two bits of state and three possible states controls a motor. The states are: `00` (stopped), `10` (slow) and `11` (fast). There are two one-bit inputs: `go` (to speed up) and `stop` (to stop).

Write the truth table corresponding to the following state transition diagram:



s: stop && !go
g: !stop && go

Your table must include the state (labelled state), the inputs (stop and go), and next state (labelled next state). You may use any of the simplification conventions described in the lecture notes, but you do not have to do this. Do not give the truth table for the output.

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This exam paper is for:

Sample Exam 2 A01234567

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told.

Name: _____

BCIT ID: _____

Signature: _____

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Question 1 — 3 marks

Fill the table below with the value of each expression as a Verilog numeric literal including the correct width and the correct value in *hexadecimal* base. Assume the following declarations:

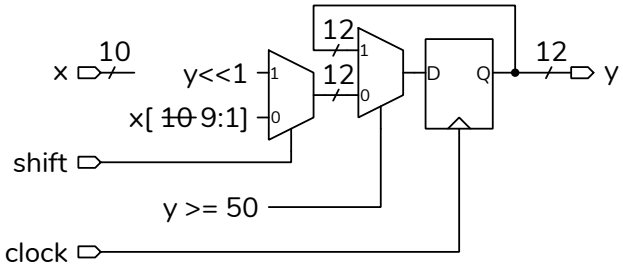
```
logic [3:0] x ;
logic [7:0] y ;
```

and that `x` has the value `4'b0110` and that `y` has the value `8'h83`. The first row has been filled in as an example. You need not show your work or draw another box around the answer.

expression	value
`y[3:0]`	`4'h3`
`y[5:0] + x * x`	
`x && ! ( 8 & y ) ^ 1`	
`~ y & 1 ? ~ ( y & 1 ) ? 0 : 1 : 2`	

Question 2 — 5 marks

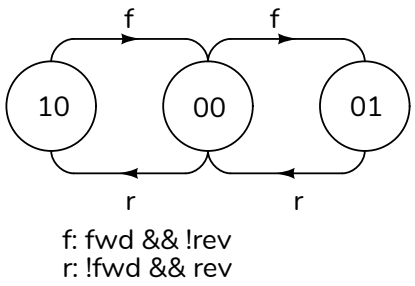
Write a Verilog module named **`adj`** that implements the following block diagram. The diagram follows the course conventions for block diagrams. Follow the course coding guidelines but omit comments.



Question 3 — 4 marks

A state machine with two bits of state and three possible states controls a motor. The states are: **`00`** (stopped), **`10`** (reversed) and **`01`** (forward). There are two one-bit inputs: **`fwd`** (forward) and **`rev`** (reverse).

Write the truth table corresponding to the following state transition diagram:



Your table must include the state (labelled state), the inputs ~~(stop and go)~~(fwd and rev), and next state (labelled next state). You may use any of the simplification conventions described in the lecture notes, but you do not have to do this. Do not give the truth table for the output.