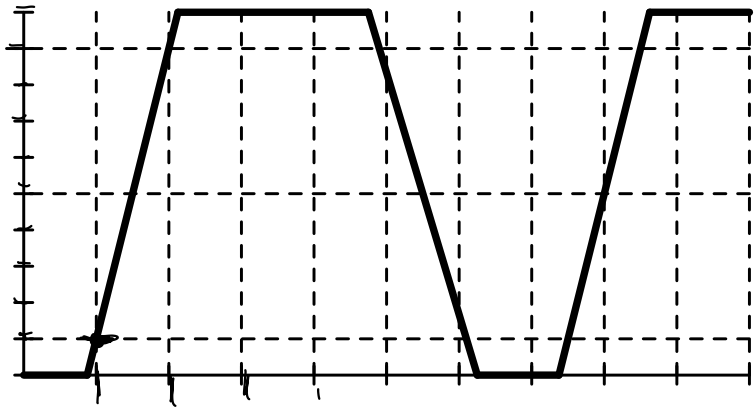
Static Timing Analysis

Exercise 1:

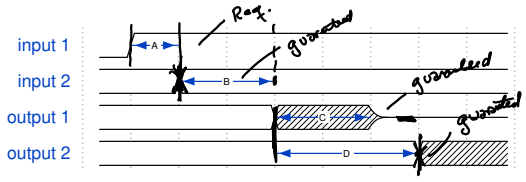


rise time = 20ns
period = 6.5 div · 20ns/div
= 130ns
+ve pulse width = 4 x 20
= 80ns
-ve " " = 2.5 x 20
= 50

The diagram above shows an oscilloscope screen capture that includes one period of an *active-low* digital waveform. The scale on the horizontal axis is 20 ns per division. What are: the rise time, period, positive pulse width and duty cycle?

duty cycle = $\frac{50}{130}$ =

Exercise 2:



Label the specifications A through D as requirements or guaranteed responses. Which specifications are measured to a signal being in a high-impedance state? Which are measured from a rising edge only? From either?

A → C → B

Exercise 3: Is t_{PD} a requirement or a guaranteed response?

Exercise 4: Is t_{SU} a requirement or a guaranteed response? How about t_H?

t_{SU} – requirement – measured to rising clock edge
t_H – requirement – measured to change in data (D)

Exercise 5:

$$t_{SU}\text{ (avail)} = T_{clock} - t_{CO}\text{ (max)} - t_{PD}\text{ (max)}$$

Which of the specifications in the formula above decrease the available setup time as they increase? Which increase it?

larger t_{CO} & t_{PD} decrease available setup time.
larger T_{clock} increases t_{SU} (avail).

Exercise 6: For a particular circuit f_{clock} is 50 MHz, t_{CO} is 2 ns (maximum), the worst-case (maximum) t_{PD} in a circuit is 15 ns and the minimum setup time requirement is 5 ns. What is the setup time slack? Will this circuit operate reliably? If not, what it the maximum clock frequency at which it will?

$f_{clock} = 50MHz$

$T_{clock} = 20ns$

$t_{su(avail)} = T_{clock} - t_{co} - t_{PD}$

$= 20 - 2 - 15 = 3ns$

$slack = t_{su(avail)} - t_{su(req'd)}$

$= 3 - 5ns = -2ns$

will not operate reliably because setup time requirement not met.

If $slack = 0$ $t_{su(avail)} = t_{su(req'd)}$

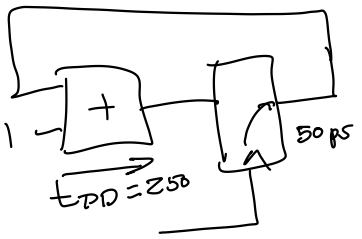
$t_{su(req'd)} = t_{su(avail)} (5ns) = T_{clock} - t_{co} - t_{PD}$

solve for $T_{clock} = t_{su(req'd)} + t_{co} + t_{PD}$

$= 5 + 2 + 15 = 22ns$

$f_{clock} = \frac{1}{T_{clock}} = \frac{1}{22ns} = 45.5\ MHz$

Exercise 7: What is the maximum clock frequency for a counter using flip-flops with 200 ps setup times, 50 ps clock-to-output delays and adder logic that has a 250 ps propagation delay?



for $slack = 0$ $t_{su(req.)} = t_{su(avail)}$

$T_{clock} = t_{su(req)} + t_{co} + t_{PD}$

$= 200 + 50 + 250 = 500ps$

$f_{clock} = \frac{1}{0.5ns} = 2\ GHz$

$= 500ps.$