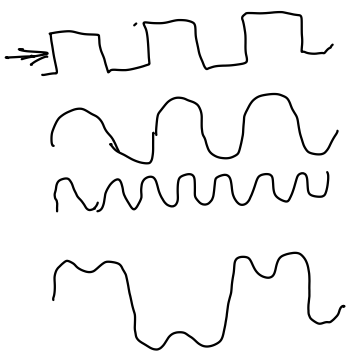
Analog Interfaces

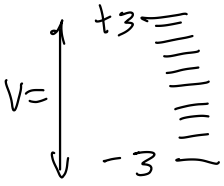
Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to be able to recover frequency components up to the 7'th harmonic (at 70 kHz)?



$f_{sample} > 2 \times 70\ kHz$

$> 140\ kHz$

Exercise 3: A signal with range of ±3 V must be quantized so that the maximum *quantization error* is less than 1 mV. What is the resolution in mV? What minimum number of bits of resolution is required?

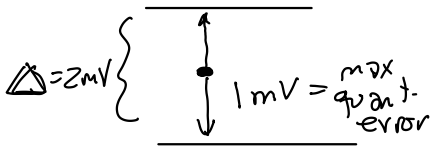


$\Delta \leq \frac{V}{2^n} = \frac{6V}{2^n} = 0.002V$

$\log_2(2^n) \geq \log_2\left(\frac{6}{0.002}\right)$

$n \geq 11.55$

use $n = 12$ bits of resolution



$\Delta < 2mV$

error $< 1mV$

Exercise 4: When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?

$n = 12$ SNR (dB) $= 1.76 + 6n = 1.76 + 6 \cdot 12$

$= 73.76$

$\frac{S}{N} = 10^{\frac{73.76}{10}}$

$\frac{S}{N} = \frac{1}{2} = 10^{\frac{x}{10}}$

$x \approx -3$

$P = V^2$

$P_1 = V_1^2$

$P_2 = V_2^2 = \left(\frac{V_1}{2}\right)^2 = \frac{V_1}{4}$

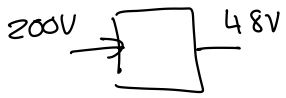
new SNR $= \left.\frac{S/4}{N}\right|_{\text{linear}} \Leftrightarrow \frac{S}{N} - 6\ dB$

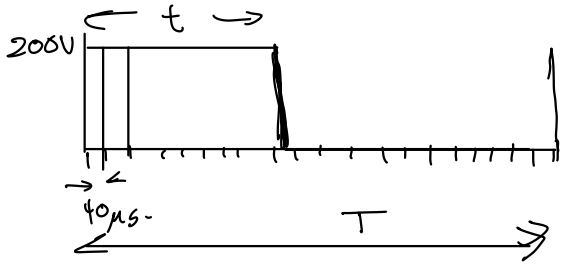
$= 74 - 6 = 68\ dB.$

also: now using 11 bits

SNR dB $= 1.76 + 6 \cdot 11 = 68\ dB$

Exercise 8: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The clock frequency is 25 kHz. What is the pulse duration?





$T_{clock} = \frac{1}{25kHz}$

$= 40\mu s$

$V_o = V_{ref} \cdot \frac{t}{T}$

$\frac{t}{T} = \frac{48}{200}$

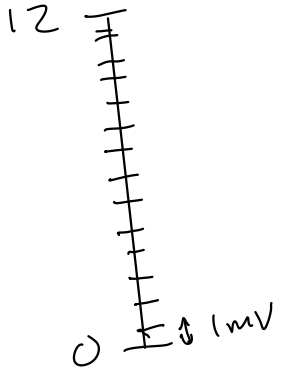
$48 = 200 \cdot \frac{t}{T}$ ✓

assume $n = 10$ $\quad 2^n = 1024$

$T = T_{clock} \cdot 2^n = 40\mu s \cdot 1024 \approx 40ms$

$t = T \cdot \frac{48}{200} = 40 \times 10^{-3} \cdot \frac{48}{200} =$

Exercise 9: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?



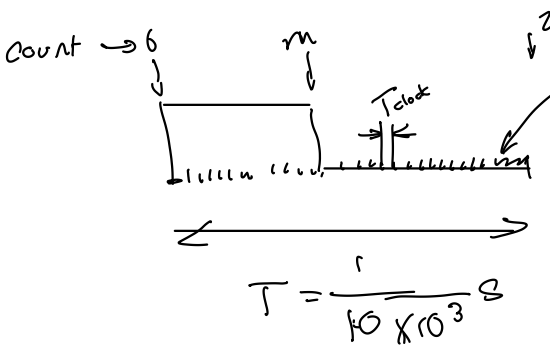
$\frac{12\,V}{1mV} = 12{,}000$

$2^n \geq 12{,}000$

$n \geq \log_2 12000$

≥ 13.5

Use $n = 14$



$T_{clock} = \frac{T}{2^n} = \frac{1}{10 \times 10^3 \cdot 2^{14}} =$

$=$

Exercise 10: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

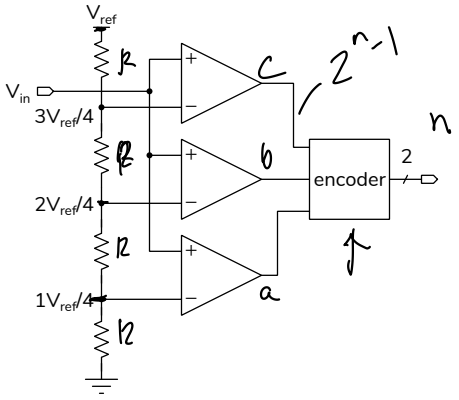
binary-weighted : $f_{sample} = f_{clock}$

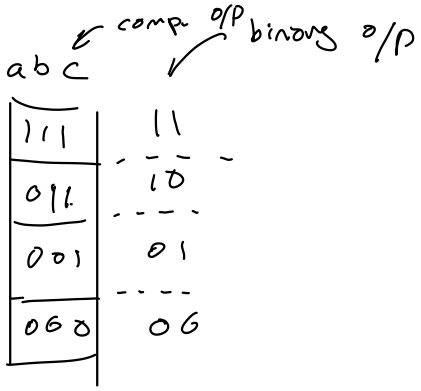
$\Sigma\Delta$: $f_{sample} \approx \frac{f_{clock}}{2^n}$

PWM DAC : $f_{sample} < \frac{f_{clock}}{2^n}$

fastest ↓ slowest

Exercise 11:

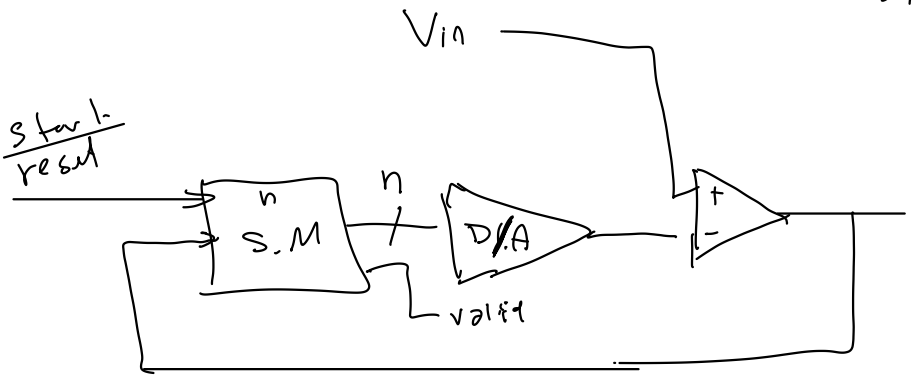




Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

Exercise 12: How many states will be required for each conversion of an n-bit SAR ADC?

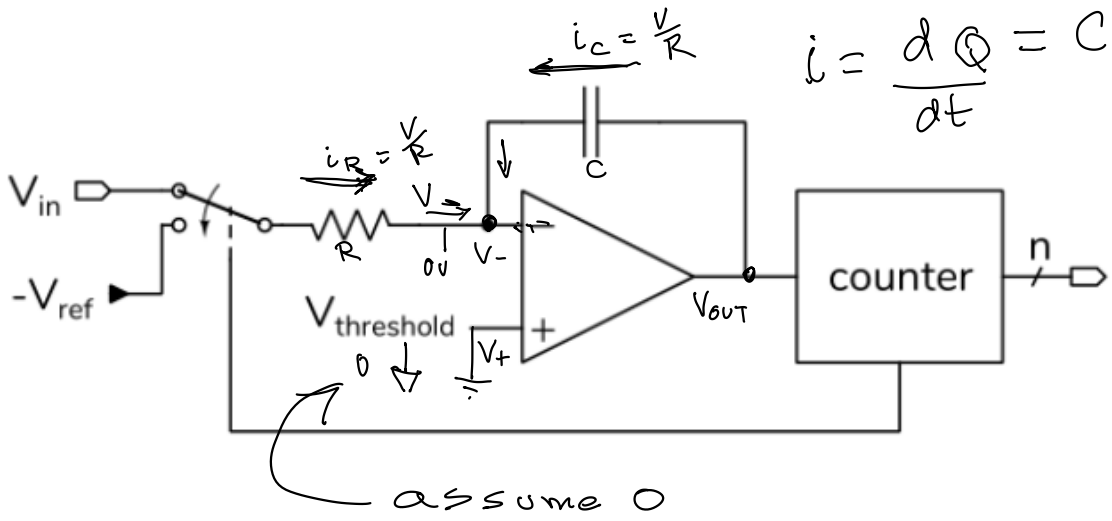
D/A = D.A.C.



4 2 1

need n clock cycles per conversion.

Exercise 14: What is the slope of an integrator, in $\mathrm{V/s}$, when charging a 100 nF capacitor with 5 V through a $100\,\mathrm{k\Omega}$ resistor?



Op-Amps 101

$V_{OUT} = A_V(V_+ - V_-)$ but $A_V \approx \infty$ $\therefore V_+ \approx V_-$

$Z_{in} = \infty$ $\therefore i_+ \approx i_- \approx 0$

$$\text{solve} = \frac{V}{RC} = \frac{5}{100\times10^{-9}\times100\times10^{3}}$$

$$= \frac{5}{10^{4}\times10^{-6}} = \frac{5}{10^{-2}} = \boxed{500\,V/s}$$