Analog Interfaces

Exercise 1:   Draw a sine wave and indicate two sets of sampling points at twice the frequency of the sine wave: one with samples at the zero crossings and one with samples at the peaks of the signal. Is it sufficient to sample at twice the highest frequency of the analog signal?

Exercise 2: What minimum sampling rate would be required to digitize a 10 kHz square wave if you wanted to be able to recover frequency components up to the 7'th harmonic (at 70 kHz)?

Exercise 3: A signal with range of ± 3 V must be quantized so that the maximum *quantization error* is less than 1 mV. What is the resolution in mV? What minimum number of bits of resolution is required?

Exercise 4:   When quantizing a full-scale sine wave, what quantization SNR would be achieved with a resolution of 12 bits? What if the signal's voltage range was only half of the full-scale range?

Exercise 5: A signal-to-noise power ratio of about 48 dB is considered "good enough" for speech communication. Assuming the formula above applies for a speech signal, approximately how many bits per sample are required to obtain this quantization SNR? If the speech signal contains frequency components up to 4 kHz, what minimum sampling rate is required? What bit rate is required to store or transmit the digitized signal?

Exercise 6: A DAC outputs a digitized 1 kHz sine-wave signal. The analog output is analyzed and the power at 1 kHz is found to be 0.5 W while the power at all other frequencies adds up to 10 mW. What is the ENOB?
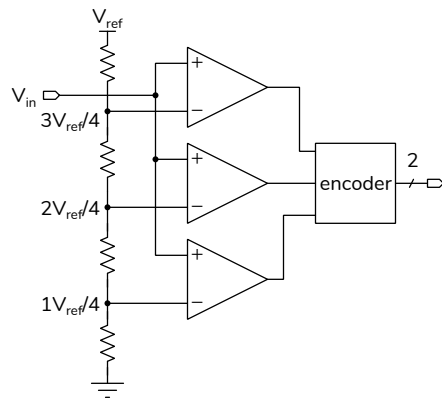
Exercise 7:
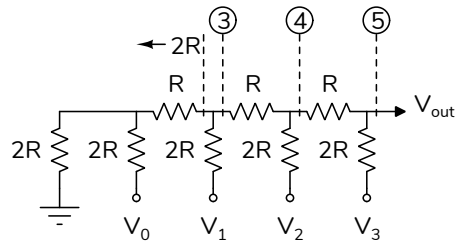
Show this. Assume V_1 is set to V_{ref} and all other inputs are zero (grounded). Find the output Thevenim resistance (resistance to ground at V_{out} with V_1 shorted) and voltage (V_{out} with $V_1 = V_{ref}$). *Hint: Do this at the labelled nodes.*

Exercise 8: You are using a PWM DAC to convert a 200 VDC supply to a 48 VDC output. The clock frequency is 25 kHz. What is the pulse duration?

Exercise 9: You are designing a PWM DAC and need resolution of 1 mV with a full-scale output of 12 V. How many bits of resolution are required? The pulse frequency is 10 kHz. What is the clock frequency?

Exercise 10: Rank the different DACs described above in terms of sampling rate relative to clock rate and complexity relative to resolution.

Exercise 11:

Draw a diagram showing the voltage ranges, the comparator outputs and the binary output for the 4-bit flash ADC above.

Exercise 12: How many states will be required for each conversion of an n-bit SAR ADC?

Exercise 13: A SAR ADC using a 4-bit DAC with a full-scale range of 0 to 7.5 V digitizes a 5.25 V signal. What voltages will the DAC output during the conversion?

Exercise 14: What is the slope of an integrator, in V/s, when charging a 100 nF capacitor with 5 V through a $100\,k\Omega$ resistor?