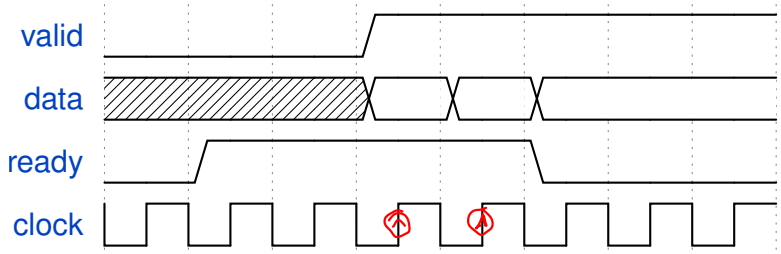
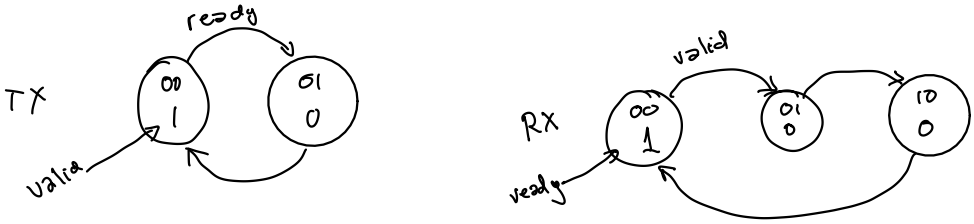
Digital Interfaces

Version 2: corrected answer to Question 4.

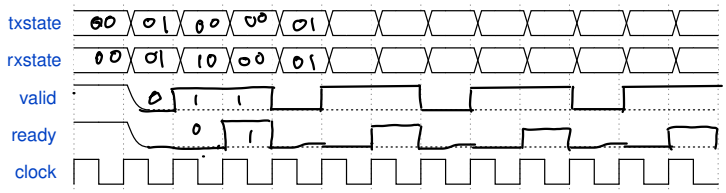
Exercise 1:



Mark the clock edges where data is transferred.

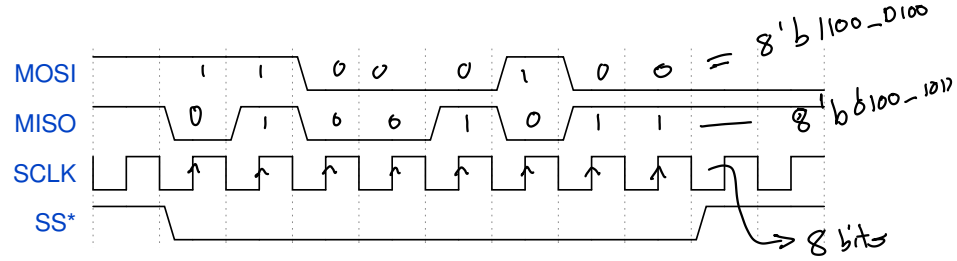


Exercise 2:



Draw the state transition diagrams for the transmitter and receiver if the transmitter has a data word ready two clock cycles after the previous one is read and the receiver requires three clock cycles to process each received word. Draw the timing diagram assuming valid and ready are asserted to start with.

Exercise 3:

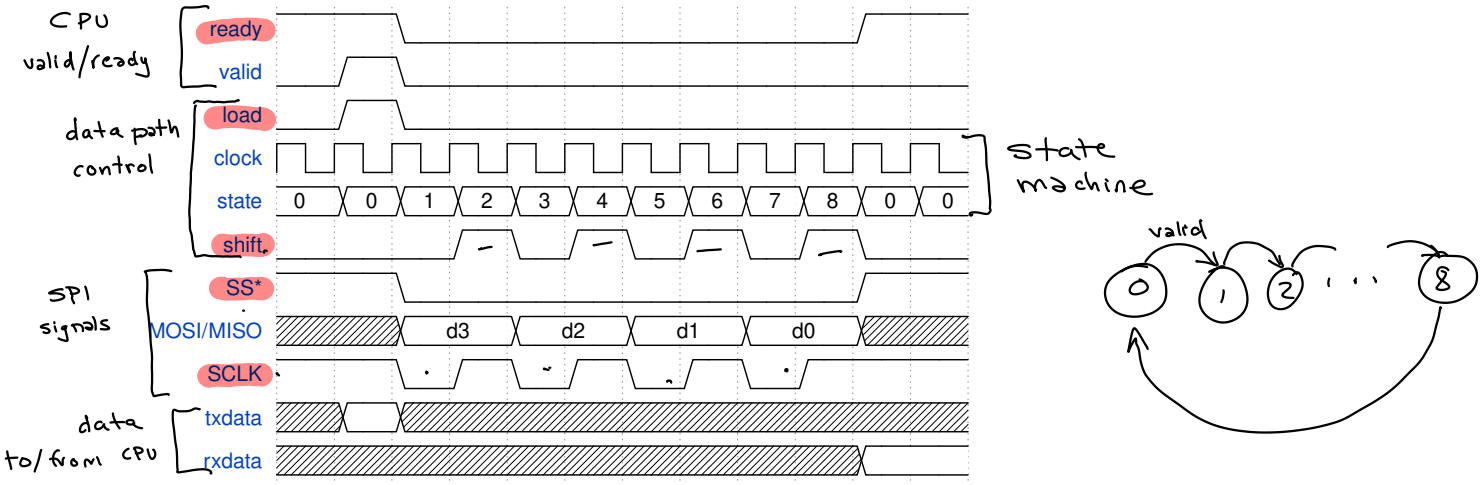


The diagram above shows a transfer over an SPI bus. How many bits of data are transferred? What is the value, in decimal, of the data transferred from the master to the slave? From the slave to the master?

8'b1100_0100 = 8'd196 — MOSI — Master to slave

8'b0100_1011 = 8'd75 — MISO — slave to master.

Exercise 4:



The diagram above shows the signals and state variable for a 4-bit SPI interface. The controller sequence generator states use a binary encoding. Write a state transition table for this state machine. Write Verilog expressions for the controller outputs.

State	valid	next state
0	1	1
8	X	0
n	X	n+1

```
assign ready = !state;
assign load = valid && ready;
assign ss_n = !state;

assign shift = state == 2 ||
               state == 4 ||
               state == 6 ||
               state == 8;

assign sclk = state == 1 ||
              state == 3 ||
              state == 5 ||
              state == 7 ? 0 : 1
```